ENGG*4560 Embedded System Design

01

Winter 2024
Section(s): 01

School of Engineering
Credit Weight: 0.75
Version 1.00 - January 12, 2024

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1 Course Details

1.1 Calendar Description

This course introduces the basic principles of embedded system design. It utilizes advanced hardware/software abstractions to help design complex systems. Topics include: design of embedded CUPs; embedded architecture cores; system-on-chip designs and integration using processor cores and dedicated core modules; embedded computing platforms; embedded programming design and analysis; processes and operating systems; networks for embedded systems; distributed embedded architectures; design examples that target robotics, automobile, and communication systems.

Pre-Requisites:	ENGG*3380 or ENGG*3640
Restrictions:	Non-BENG students may take a maximum of 4.00 ENGG credits.

1.2 Course Description

This course is a senior-level course in electrical and computer engineering and introduces basic principles of embedded systems design. Topics include:

- Hardware description language for embedded system design and simulation.
- System-on-chip design and integration using processor cores and dedicated hardware core modules.
- On-chip busses and bus protocols.
- Hardware/software interfaces.
- Coprocessor design and analysis.
- Embedded computing platforms.
- Applications: design of security components for embedded systems.

1.3 Timetable

Lectures

Tuesday Sec 01: 2:30 pm – 3:50 pm; Room MCKN 223

Thursday Sec 01: 2:30 pm – 3:50 pm; Room MCKN 223

Laboratory

Friday Sec 01: 8:30 am – 11:20 am; Room RICH 1532

1.4 Final Exam

April 23, 2024 (Tuesday): 11:30 am – 1:30 pm; Type: in-class; Room: TBA

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2 Instructional Support

2.1 Instructional Support Team

Instructor:	Radu Muresan Ph.D., P.Eng.
Email:	rmuresan@uoguelph.ca
Telephone:	+1-519-824-4120 x56730
Office:	RICH 2509
Office Hours:	Thursday: 4 pm - 5 pm
Lab Technician:	Kevin Dong
Email:	kdong@uoguelph.ca
Office:	RICH 2506

2.2 Teaching Assistants

Teaching Assistant (GTA):	Pranjali Suresh Sagar
Email:	psagar@uoguelph.ca
Office:	TBA
Office Hours:	TBA

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3 Learning Resources

3.1 Required Resources

Course Website (Website)

Course material, news, announcements, and grades will be regularly posted to the ENGG*4560 CourseLink site. You are responsible for checking the course site regularly.

[1] ENGG4560 Lecture Notes, W23 Version (Notes)
ENGG*4560 W23 CourseLink, University of Guelph, Radu Muresan

[2] ENGG4560 Laboratory Manual, W23 Version (Lab Manual)
ENGG4560 W23 CourseLink, University of Guelph, Radu Muresan

[3] Verilog Tutorial (Website)
https://www.chipverify.com/verilog/verilog-tutorial

[4] DE1-SOC (Other)
https://www.intel.com/content/www/us/en/programmable/support/training/university/boards.html

[5] A Practical Introduction to Hardware/Software Codesign (Textbook)
P. R. Schaumont, Springer, 2013

[6] The Block Cipher Companion (Textbook)
L. R. Knudsen, M. J. B Robshaw, Springer 2011

[7] Advanced Encryption Standard (AES) (Article)
•NIST, FIPSP 197, 2001.

[8] Recommendation for Block Cipher Modes of Operation (Article)
NIST, 2001

[9] Avalon Interface Specifications (Other)
Intel, 2022 Version

[10] AMBA APB Protocol Specification (Other)
ARM, 2021 Version

[11] AMBA AXI and ACE Protocol Specification (Other)
ARM, 2021 Version

3.2 Recommended Resources

[7] Introduction to Cryptography (Textbook)
Alexander Stanoyevitch, CRC Press, 2013

3.3 Additional Resources

Additional Resources (Other)

Lecture Information: All lecture notes are posted on the ENGG*4560 CourseLink system (Week #1 to Week #12) in Content/LECTURES module.

Lab Information: The ENGG*4560 Embedded Systems Design Lab Manual is posted on the ENGG*4560 CourseLink system in Content/LABORATORY module.

Assignments: Practice Exam Questions and Problems: ENGG*4560 CourseLink system in the Content/EXAM PROBLEMS module.

Exams: Some example solutions of previous final exams: ENGG*4560 CourseLink system in the Content/EXAM PROBLEMS module.

Miscellaneous Information: Other information related to embedded systems design will be posted on the course home announcements.

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4 Learning Outcomes

4.1 Course Learning Outcomes

By the end of this course, you should be able to:

1. Use of mainstream HDL such as Verilog, VHDL, or SystemC
2. Design simple system-on-chip hardware components using HDL
3. Design complex system-on-chip applications with hardware processor and FPGA cores (DE1-SOC Architecture)
4. System-on-chip design concepts
5. On-chip busses and bus protocols
6. Design Hardware/Software Interfaces
7. Coprocessor design concepts and example applications
8. Design security components for embedded systems
9. Explore and present new research results in the field of embedded systems design through reports and presentations
10. Use of embedded systems design tools

4.2 Engineers Canada - Graduate Attributes (2018)

Successfully completing this course will contribute to the following:

#	Outcome	Learning Outcome
1	Knowledge Base	4, 5, 6, 7, 8
1.4	Recall, describe and apply program-specific engineering principles and concepts	4, 5, 6, 7, 8
2	Problem Analysis	1, 2, 3, 4, 5, 6, 7, 8, 10
2.3	Construct a conceptual framework and select an appropriate solution approach	1, 10
2.4	Execute an engineering solution	1, 2, 3, 4, 5, 6, 7, 8, 10
4	Design	1, 2, 3, 4, 5, 6,

#	Outcome	Learning Outcome
		7, 8, 10
4.3	Create a variety of engineering design solutions	1, 2, 3, 4, 5, 6, 7, 8, 10
5	Use of Engineering Tools	1, 2, 3, 10
5.2	Demonstrate proficiency in the application of selected engineering tools	1, 2, 3, 10
6	Individual & Teamwork	3, 6, 7, 8, 9, 10
6.1	Describe principles of team dynamics and leadership	3, 6, 7, 8, 9, 10
6.2	Understand all members' roles and responsibilities within a team	3, 6, 7, 8, 9, 10
6.3	Execute and adapt individual role to promote team success through, for example, timeliness, respect, positive attitude	3, 6, 7, 8, 9, 10
7	Communication Skills	9
7.1	Identify key message(s) and intended audience in verbal or written communication as both sender and receiver	9
7.2	Interpret technical documentation such as device specification sheets, drawings, diagrams, flowcharts, and pseudocode	9
7.3	Construct the finished elements using accepted norms in English, graphical standards, and engineering conventions, as appropriate for the message and audience	9
7.4	Substantiate claims by building evidence-based arguments and integrating effective figures, tables, equations, and/or references	9
7.5	Demonstrate ability to process oral and written communication by following instructions, actively listening, incorporating feedback, and formulating meaningful questions	9

5 Teaching and Learning Activities

The course activities are given in weeks. The total number of weeks of classes for this term is 12. Therefore, the week number indicated for the activities in this section refers to the weeks

of active classes, not the weeks of the semester.

5.1 Lecture

Week 1-2

Topics:	HDL Basics, Verilog primer for system on chip design
References:	[1], [2], [3]
Learning Outcome:	1, 2

Week 3

Topics:	SoC FPGA Devices, DE1-SOC Architecture
References:	[1], [2], [4]
Learning Outcome:	3

Week 3-6

Topics:	Embedded systems design, system-on-chip design concepts: 1. SoC (System on Chip) design principles 2. On-chip busses 3. Hardware/software interfaces 4. AES coprocessor design analysis and examples
References:	[1], [2], [5]
Learning Outcome:	4, 5, 6, 7, 8

Week 7-11

Topics:	Applications : Design of security components for embedded systems 1. Block cipher design and integration: AES 2. Integration of ciphers as security components in

embedded systems

3. Standard SoC interface protocols: Avalon and AMBA APB and AXI

References: [1], [2], [5], [7-11]

Learning Outcome: 5, 6, 7, 8

Week 12

Topics: Current trends in embedded systems design, research survey paper development

Learning Outcome: 9

5.2 Lab

Week 1

Topics: LAB 0: Safety and Group Formation

References: [2]

Week 1-3

Topics: Laboratory 1: Design Simple FPGA Circuits in Verilog

References: [2]

Learning Outcome: 1, 2, 3, 10

Week 1: Tools presentation and laboratory presentation

Week 2: Laboratory development -- in class work

Week 3: Laboratory development plus laboratory demo; Lab 2 presentation

Week 4-5

Topics: Laboratory 2: Design FPGA Circuits with Verilog, Schematics and IPs

References: [2]

Learning Outcome: 1, 2, 3, 10

Week 4: Laboratory presentation plus laboratory development

Week 5: Laboratory development plus laboratory demo; Lab 3 presentation

Week 6-7

Topics: Laboratory 3: HPS and FPGA Design Using Memory Mapping Technique

References: [6]

Learning Outcome: 1, 2, 3, 10

Week 6: Laboratory presentation plus laboratory development

Week 7: Laboratory development plus laboratory demo

Week 8- 12

Topics: Laboratory 4/Project: Design the AES Coprocessor working in CBC or OFB mode using Memory-Mapped interface technique

References: [6]

Learning Outcome: 1, 3, 5, 6, 7, 8, 10

The laboratory 4/project component includes a demo of the implementation and a final complete report (minimum 8 pages and maximum 10 pages, font size 12 Time Romans); Sections of the report should include: Introduction, Background and Theory, Methodology, Results and Analysis, Conclusions, and References. Your report must detail your overall block diagram and explain the overall components design and functionality. Analyse the performance of the implementation and discuss possible improvements.

Project development schedule:

Week 8: Laboratory presentation and development

Week 9: Laboratory development

Week 10: Laboratory progress demo

Week 11: Laboratory development

Week 12: Laboratory demo plus laboratory report submission

5.3 Other Important Dates

You can refer the student undergraduate calendars for the semester scheduled dates.

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6 Assessments

Please be advised that the "Marking Schemes & Distribution" Table in Section 6.1 is conditional on the final exam score. Consult Section 6.1 for all marking conditions!

6.1 Marking Schemes & Distributions

Passing course conditions:
1. The students must pass all labs (demos and reports), and each student must be part of the laboratory demo. If a student misses a laboratory demo, a makeup lab demo must be arranged by week 12 of the semester.
2. The students must obtain a passing mark on the research survey paper.
3. Students must write a final exam or a deferred final exam. If a student does not meet all of the above conditions (1, 2, and 3), the final course mark will be 47%. When the above conditions (1, 2, and 3) are all met, the final course mark calculation follows two marking schemes, which depend on the final exam result. Specifically, when the result in the final exam is a passing mark (>=50%), the course marking Scheme A is applied, and when the result in the final exam is a failing mark (<50%) the course marking Scheme B is applied.

Name	Scheme A (%)	Scheme B (%)
Labs + Project	45	40
Research Survey Paper	15	10
Final Exam	40	50
Total	100	100

6.2 Assessment Details

Labs (45%)

Learning Outcome: 1, 2, 3, 6, 7, 8, 10
Laboratory 1, Laboratory 2, and Laboratory 3 have only a demo that is worth 5%, 5%, and 8%, respectively (See due dates in Laboratory Activity section).

Laboratory4/Project has a laboratory progress design demo, a final laboratory/project demo and a final laboratory/project report (See due dates in Laboratory Activity section).

The laboratory 4/project is marked as follows: laboratory progress demo is worth 5%, final laboratory 4/project demo is worth 10%, and the laboratory 4/project report is worth 12%

Research Survey Paper (15%)

Date: Week 12
Learning Outcome: 9

Current topics in embedded systems design, research paper survey (Due date: Thursday, Week 12 of classes)

This research survey paper is weighted to 15% of the final course mark and is a group report in a conference IEEE paper format.

- This research report should be a survey on current embedded systems design topics. The paper must be developed following the paper survey samples posted on CourseLink. The paper length should be five pages, and the paper should follow the IEEE conference paper format and style (see sample papers on CourseLink.

Final Exam (40%)
Date: Tue, Apr 23, 11:30 AM - 1:30 AM, TBA
Learning Outcome: 1, 2, 2, 3, 4, 5, 6, 7, 8
Final Exam: The weight of the final exam is conditional on the final mark obtained in the exam (See Marking Schemes Table). The final exam will cover the entire course material, with some exceptions that will be posted on CourseLink.

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7 Course Statements

7.1 Course Grading Policies

Missed Assessments: If you are unable to meet an in-course requirement due to medical, psychological, or compassionate reasons, please email the course instructor. See the undergraduate calendar for information on regulations and procedures for Academic Consideration:
http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-ac.shtml

Accommodation of Religious Obligations: If you are unable to meet an in-course requirement due to religious obligations, please email the course instructor at the start of the semester to make alternate arrangements. See the undergraduate calendar for information on regulations and procedures for Academic Accommodation of Religious Obligations:
http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-accomrelig.shtml

Passing grade: Passing course conditions:
1. The students must pass all labs (demos and reports), and each student must be part of the laboratory demo. If a student misses a laboratory demo, a makeup lab demo must be arranged by week 12 of the semester.
2. The students must obtain a passing mark on the research survey paper.
3. The students must write the final exam.
If a student does not meet all of the above conditions (1, 2, and 3), the final course mark will

be 47%.
When the above conditions (1, 2, and 3) are all met, the final course mark calculation follows two marking schemes, which depend on the final exam result. Specifically, when the result in the final exam is a passing mark (>=50%), the course marking Scheme A is applied, and when the result in the final exam is a failing mark (<50%) the course marking Scheme B is applied.

Lab/Project Work: You must attend all lab demos and complete all lab reports. However, suppose you miss a laboratory demo due to grounds for granting academic consideration or religious accommodation. In that case, arrangements must be made with the instructor to complete a makeup lab demo by week 12 of the semester.

Late Lab/Project Reports: Late submissions of lab reports will be accepted only with the approval of the course instructor. However, penalties for late submissions might be applied. Applied penalties will be posted on the ENGG*4560 CourseLink system.

7.2 Relationships with other Courses & Labs

Previous Courses:

ENGG*3640 (Microcomputer Interfacing): instruction set architecture, microcontroller architecture and design, interfacing principles and components.

ENGG*3380 (Computer Organization and Design): CPU design, instruction set design, microprocessor architectures and design, interfacing principles and components.

8 School of Engineering Statements

8.1 Instructor's Role and Responsibility to Students

The instructor’s role is to develop and deliver course material in ways that facilitate learning for a variety of students. Selected lecture notes will be made available to students on Courselink but these are not intended to be stand-alone course notes. Some written lecture notes will be presented only in class. During lectures, the instructor will expand and explain the content of notes and provide example problems that supplement posted notes. Scheduled classes will be the principal venue to provide information and feedback for tests and labs.

8.2 Students' Learning Responsibilities

Students are expected to take advantage of the learning opportunities provided during lectures and lab sessions. Students, especially those having difficulty with the course content, should also make use of other resources recommended by the instructor. Students who do (or may) fall behind due to illness, work, or extra-curricular activities are advised to keep the instructor informed. This will allow the instructor to recommend extra resources in a timely manner and/or provide consideration if appropriate.

8.3 Lab Safety

Safety is critically important to the School and is the responsibility of all members of the School: faculty, staff and students. As a student in a lab course you are responsible for taking all reasonable safety precautions and following the lab safety rules specific to the lab you are working in. In addition, you are responsible for reporting all safety issues to the laboratory supervisor, GTA or faculty responsible.

9 University Statements

9.1 Email Communication

As per university regulations, all students are required to check their e-mail account regularly: e-mail is the official route of communication between the University and its students.

9.2 When You Cannot Meet a Course Requirement

When you find yourself unable to meet an in-course requirement because of illness or compassionate reasons please advise the course instructor (or designated person, such as a teaching assistant) in writing, with your name, id#, and e-mail contact. The grounds for Academic Consideration are detailed in the Undergraduate and Graduate Calendars.

Undergraduate Calendar - Academic Consideration and Appeals
https://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-ac.shtml

Graduate Calendar - Grounds for Academic Consideration
https://www.uoguelph.ca/registrar/calendars/graduate/current/genreg/index.shtml

Associate Diploma Calendar - Academic Consideration, Appeals and Petitions
https://www.uoguelph.ca/registrar/calendars/diploma/current/index.shtml

9.3 Drop Date

Students will have until the last day of classes to drop courses without academic penalty. The deadline to drop two-semester courses will be the last day of classes in the second semester. This applies to all students (undergraduate, graduate and diploma) except for Doctor of Veterinary Medicine and Associate Diploma in Veterinary Technology (conventional and alternative delivery) students. The regulations and procedures for course registration are available in their respective Academic Calendars.

Undergraduate Calendar - Dropping Courses
https://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-drop.shtml

Graduate Calendar - Registration Changes
https://www.uoguelph.ca/registrar/calendars/graduate/current/genreg/genreg-reg-regchg.shtml

Associate Diploma Calendar - Dropping Courses
https://www.uoguelph.ca/registrar/calendars/diploma/current/c08/c08-drop.shtml

9.4 Copies of Out-of-class Assignments

Keep paper and/or other reliable back-up copies of all out-of-class assignments: you may be asked to resubmit work at any time.

9.5 Accessibility

The University promotes the full participation of students who experience disabilities in their academic programs. To that end, the provision of academic accommodation is a shared responsibility between the University and the student.

When accommodations are needed, the student is required to first register with Student Accessibility Services (SAS). Documentation to substantiate the existence of a disability is required; however, interim accommodations may be possible while that process is underway.

Accommodations are available for both permanent and temporary disabilities. It should be noted that common illnesses such as a cold or the flu do not constitute a disability.

Use of the SAS Exam Centre requires students to make a booking at least 14 days in advance, and no later than November 1 (fall), March 1 (winter) or July 1 (summer). Similarly, new or changed accommodations for online quizzes, tests and exams must be approved at least a week ahead of time.

For Guelph students, information can be found on the SAS website
https://www.uoguelph.ca/sas

For Ridgetown students, information can be found on the Ridgetown SAS website
https://www.ridgetownc.com/services/accessibilityservices.cfm

9.6 Academic Integrity

The University of Guelph is committed to upholding the highest standards of academic integrity, and it is the responsibility of all members of the University community-faculty, staff, and students-to be aware of what constitutes academic misconduct and to do as much as possible to prevent academic offences from occurring. University of Guelph students have the responsibility of abiding by the University's policy on academic misconduct regardless of their location of study; faculty, staff, and students have the responsibility of supporting an environment that encourages academic integrity. Students need to remain aware that instructors have access to and the right to use electronic and other means of detection.

Please note: Whether or not a student intended to commit academic misconduct is not relevant for a finding of guilt. Hurried or careless submission of assignments does not excuse students from responsibility for verifying the academic integrity of their work before submitting it. Students who are in any doubt as to whether an action on their part could be construed as an academic offence should consult with a faculty member or faculty advisor.

Undergraduate Calendar - Academic Misconduct
https://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-amisconduct.shtml

Graduate Calendar - Academic Misconduct
https://www.uoguelph.ca/registrar/calendars/graduate/current/genreg/index.shtml

9.7 Recording of Materials

Presentations that are made in relation to course work - including lectures - cannot be recorded or copied without the permission of the presenter, whether the instructor, a student, or guest lecturer. Material recorded with permission is restricted to use for that course unless further permission is granted.

9.8 Resources

The Academic Calendars are the source of information about the University of Guelph's procedures, policies, and regulations that apply to undergraduate, graduate, and diploma programs.

Academic Calendars
https://www.uoguelph.ca/academics/calendars

9.9 Illness

Medical notes will not normally be required for singular instances of academic consideration, although students may be required to provide supporting documentation for multiple missed assessments or when involving a large part of a course (e.g.. final exam or major assignment).
