ENGG*4550 VLSI Digital Design

01

Winter 2024
Section(s): C01

School of Engineering
Credit Weight: 0.50
Version 1.00 - January 07, 2024

---

1 Course Details

1.1 Calendar Description

This course introduces the students to the analysis, synthesis and design of Very Large Scale integration (VLSI) digital circuits and implementing them in silicon. The topics of this course are presented at three levels of design abstraction. At device level: MOS diode; MOS (FET) transistor; interconnect wire. At circuit level: CMOS inverter; static CMOS gates (NAND, NOR); dynamic gates (NAND, NOR); static latches and registers; dynamic latches and registers; pipelining principles and circuit styles; BICMOS logic circuits. At system level; implementation strategies for digital ICs; interconnect at system level; timing issues in digital circuits (clock structures); the adder; the multiplier; the shifter; memory design and array structure; low power design circuits and architectures.

Pre-Requisites:	ENGG*2410, ENGG*2450, ENGG*3450
Restrictions:	This is a Priority Access Course. Enrolment may be restricted to the CENG specialization in the BENG and BENG:C programs. See department for more information. Non-BENG students may take a maximum of 4.00 ENGG credits.

1.2 Course Description

This course is a senior level course in electrical and computer engineering. The main goals of the course are: (1) to teach students the fundamentals of the VLSI digital design at all levels of design abstraction (i.e., physical design, circuit design, logic design, microarchitecture design, and architecture design), (2) to teach students the importance of the key factors in the VLSI design (i.e., delay, power, interconnect, and robustness).

1.3 Timetable

Lectures

Monday 4:00 PM – 5:20 PM, MCKN 224

Wednesday 4:00 PM – 5:20 PM, MCKN 224

Laboratory

Friday Section 1 - 2:30 PM - 4:20 PM - RICH 2531

Monday Section 2 - 8:30 AM - 10:20 AM - RICH 2531

1.4 Final Exam

Final Exam:

April 20th, 2024: 8:30 AM to 10:30 AM

Exam time and location are subject to change. Please see WebAdvisor for the latest information.

---

2 Instructional Support

2.1 Instructional Support Team

Instructor: Ahmed Refaey Hussein Ph.D., PEng.
Email: ahmed@uoguelph.ca
Telephone: 519-824-4120 X52506
Office: THRN 2409
Office Hours: online by appointment
Students can come for consultations during my office hours or can make an appoinment as necessary

Lab Co-ordinator: Haleh Vahedi
Email: hvahedi@uoguelph.ca
Office Hours:

2.2 Teaching Assistants

Teaching Assistant (GTA): Yahuza Bello
Email: ybello@uoguelph.ca

---

3 Learning Resources

3.1 Required Resources

Course Website (Website)
Course material, news, announcements, and grades will be regularly posted to the ENGG*4550 CourseLink site and on my personal course webpage. You are responsible for checking the sites regularly.

[1] CMOS VLSI Design A Circuits and System Perspective (Textbook)
Neil H. E. Weste, David M. Harris, 4thEdition, Addison Wesley, 2011.

[2] ENGG4550 VLSI Digital Design Lab Manual (Lab Manual)
Radu Muresan, University of Guelph, 2017 Edition.

3.2 Recommended Resources

[3] CMOS Circuit Design, Layout, and Simulation (Textbook)
R. Jacob Baker, 3rd Edition (IEEE Press Series on Microelectronic System), 2010.

[4] Digital Integrated Circuits A Design Perspective (Textbook)
Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Edition, Pearson, 2003.

3.3 Additional Resources

Additional Resources (Other)
Lecture Information: All lecture notes are posted on the ENGG*4550 CourseLink system (Week #1 to Week #12) under LECTURES module.

Lab Information: The ENGG4550 VLSI Digital Design Lab Manual is posted on the ENGG*4550 CourseLink system under the LABORATORY module.

Assignments: The assignments are posted on the ENGG*4550 CourseLink system under the ASSINGMENTS module.

Exams: Some solutions of previous midterm exams will be posted on the ENGG*4550 CourseLink system under the EXAM SOLUTIONS section. Also, after the midterm exam a complete solution of the exam with the marking scheme applied will be posted for your reference.

Miscellaneous Information: Other information related to VLSI digital design systems will be posted on the web page.

---

4 Learning Outcomes

4.1 Course Learning Outcomes

By the end of this course, you should be able to:

1. Understand the MOS transistor theory and MOS transistor models for VLSI design.
2. Understand the CMOS process technology and the CMOS chip fabrication rules and steps.
3. Use chip design metrics such as delay, speed, power and robustness for VLSI designs.
4. Analyze and evaluate power at various levels of design abstraction in VLSI integrated chips.
5. Model the interconnect and basic components.
6. Design combinational and sequential circuits.
7. Design datapath subsystems such as adders, comparators, and multipliers.
8. Understand the basics of memory design for SRAM, DRAM and ROM.
9. Use simulation and fabrication tools for nanoscale VLSI designs.
10. Design gates and datapath subsystem using 45 nm CMOS technology process.
11. Demonstrate and communicate VLSI system design results.

4.2 Engineers Canada - Graduate Attributes (2018)

Successfully completing this course will contribute to the following:

#	Outcome	Learning Outcome
1	Knowledge Base	1, 2, 3, 4, 5, 6, 7, 8
1.4	Recall, describe and apply program-specific engineering principles and concepts	1, 2, 3, 4, 5, 6, 7, 8
2	Problem Analysis	2, 3, 4, 5, 6, 7, 8, 9
2.4	Execute an engineering solution	2, 3, 4, 5, 6, 7, 8, 9
4	Design	6, 7, 8, 9, 10
4.3	Create a variety of engineering design solutions	6, 7, 8, 9, 10
4.5	Develop and refine an engineering design solution, through techniques such as iteration, simulation and/or prototyping	9, 10
5	Use of Engineering Tools	9, 10
5.2	Demonstrate proficiency in the application of selected engineering tools	9, 10

#	Outcome	Learning Outcome
7	Communication Skills	11
7.3	Construct the finished elements using accepted norms in English, graphical standards, and engineering conventions, as appropriate for the message and audience	11
7.4	Substantiate claims by building evidence-based arguments and integrating effective figures, tables, equations, and/or references	11

5 Teaching and Learning Activities

5.1 Lecture

Week 1

Topics: Introduction and CMOS circuit overview

References: [1] Chapters 1, 2

Learning Outcome: 1

Week 2

Topics: Fabrication and layout, MOS transistor theory

References: Chapters 1, 2

Learning Outcome: 2, 3

Week 3

Topics: MOS Transistor I-V Characteristics and Parasitics

References: Chapter 2,3

Learning Outcome: 3

Week 4

Topics: DC & Transient Responses, gate delay models

References: Chapter 4

Learning Outcome: 3, 4

Week 5

Topics: Power: dynamic, static

References: Chapter 5

Learning Outcome: 3, 5

Week 6-7

Topics: Power: optimization, and low power architectures

References: Chapter 5

Learning Outcome: 3, 4, 6

Week 8

Topics: Interconnect: modeling and impact

References: Chapter 6

Learning Outcome: 3, 4, 6

Week 9

Topics: Combinational Circuit Design

References: Chapter 9

Learning Outcome: 3, 4, 7

Week 10

Topics: Sequential Circuit Design

References: Chapter 10

Learning Outcome: 3, 4, 7

Week 11

Topics: Arrays: SRAM, DRAM, ROM, CAM, PLAs

References: Chapter 12

Learning Outcome: 3, 4, 8

Week 12

Topics:	Robustness and Scaling (if time permits)
References:	Chapter 7
Learning Outcome:	7
Topics:	Extra Topics
	Please note that lecture topics and orders are subject to changes.
	All updated information will be posted reguraly on the course webpage.

5.2 Lab

Week 1

Topics:	Introduction to Lab Equipment and Safety Training. Introduction to Lab 1 design requirements and Cadence simulation tools
References:	[1], [2]
Learning Outcome:	1, 3, 9

Week 1-3

Topics:	Lab 1: NMOS and PMOS models. Implementation, demo and report
References:	[1], [2]
Learning Outcome:	1, 3, 9, 11

Week 3: Demo Due

Week 3: Report Due

Week 3

Topics:	Introduction to Lab 2: Logical effort simulation

References: [1], [2]

Learning Outcome: 3, 6, 9

Week 4-5

Topics: Lab 2: Logical Effort Simulation. Implementation, demo and report.

References: [1], [2]

Learning Outcome: 3, 6, 9, 11

Week 5: Demo Due

Week 5: Report Due

Week 5

Topics: Introduction to Lab 3: Layout logic cells using the 45 nm CMOS process, LVS, DRC, post layout simulation and verification

References: [1], [2]

Learning Outcome: 2, 3, 6, 9, 10

Week 6-7

Topics: Lab 3: Layout Logic Cells Using the 45 nm Process, LVS, DRC, post layout simulation and verification. Implementation, demo and report

References: [1], [2]

Learning Outcome: 2, 3, 6, 9, 10, 11

Week 7: Demo Due

Week 7: Report Due

Week 7

Topics: Introduction to Lab 4/Project: Design a pipeline stage performing ALU operations; circuit simulations and analysis report

References: [1], [2]

Learning Outcome: 2, 3, 6, 7, 9, 10

Week 8-11

Topics: Project: Program Counter. Implementation, demo, report.

Learning Outcome: 2, 3, 6, 7, 9, 10, 11
Week 11: Demo Due

Week 11: Report Due

---

6 Assessments

6.1 Marking Schemes & Distributions

Name	Scheme A (%)
Labs and Project	25
Midterm Exam	25
Final Exam	35
Practice	15
Total	100

6.2 Assessment Details

Labs and Project (25%)
Learning Outcome: 1, 2, 3, 4, 5, 6, 7, 9, 10, 11
Lab 1, lab 2, and (lab 3) total 15%

Project (lab 4) worth 10%

Midterm Exam (25%)
Date: Feb. 28th, 2024: 4pm – 5:20pm, In class
Learning Outcome: 1, 2, 3, 4

Final Exam (35%)
Date: April 20th, 2024: 8:30 am to 10:30 am, TBD
Learning Outcome: 1, 2, 3, 4, 5, 6, 7, 8

Practice (15%)
Learning Outcome: 1, 2, 3, 4, 8, 11

---

7 Course Statements

7.1 Course Grading Policies

Missed Assessments: If you are unable to meet an in-course requirement due to medical, psychological, or compassionate reasons, please email the course instructor. See the undergraduate calendar for information on regulations and procedures for Academic Consideration:
http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-ac.shtml

Accommodation of Religious Obligations: If you are unable to meet an in-course requirement due to religious obligations, please email the course instructor at the start of the semester to make alternate arrangements. See the undergraduate calendar for information on regulations and procedures for Academic Accommodation of Religious Obligations:
http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-accomrelig.shtml

Passing grade: In order to pass the course, you must meet the following conditions:

1. Students must finalize and submit all the labs and projects (Demo + Report) and obtain a passing grade of 50% or higher in all the labs and projects. If an overall grade of lower than 50% is obtained in any lab, the students need to arrange with the instructor a new demo and report submission. In this case, a grade penalty of 10% deduction will be applied.
2. Students must write both exams (midterm and final) to pass the course. If the student misses the midterm exam (with an acceptable excuse as per the university guidelines), the load will be carried to the final exam (*No makeup for the midterm*).

Contesting Marks: All laboratory and midterm exam marks must be contested within 2 days from grade submission.

Missed midterm exam: If you miss a test due to grounds for granting academic consideration or religious accommodation, the load will be carried to the final exam (*No makeup for the midterm*).

Lab Work: You must attend and complete all laboratories. If you miss a laboratory demo due to grounds for granting academic consideration or religious accommodation, arrangements must be made with the instructor to complete a makeup lab demo.

Late Lab Reports: Late submissions of lab reports will be accepted only with the approval of the course instructor. However, penalties for late submissions will be applied. Applied

penalties will be posted on ENGG*4550 CourseLink system.

Late Assessment Submission: Late submissions of assignments or activities will be penalized 10% deduction per day.

7.2 Relationships with other Courses & Labs

Previous Courses:

ENGG*2410 (Digital Systems Design Using Descriptive Language): Boolean algebra, design synthesis and realization of combinational and sequential circuits, hardware testing.

ENGG*2450 (Electric Circuits): Fundamentals of electric circuit analysis, circuit elements, DC current analysis, linearity and superposition principles, circuit theorems.

ENGG*3450 (Electrical Devices): Semiconductor materials, diodes, transistors, electronic components and circuit analysis.

7.3 Arrangements for Face-to-Face Components

1. Depending on the University's approval (*i.e.* University closure due to COVID), all labs and the project will be ONLINE or might be canceled. In case of canceling labs and the project, the scale will be distributed equally to the other course components.
2. The midterm exam will take place IN CLASS.
3. The final exam will take place in person on the advertised date.

8 School of Engineering Statements

8.1 Instructor's Role and Responsibility to Students

The instructor’s role is to develop and deliver course material in ways that facilitate learning for a variety of students. Selected lecture notes will be made available to students on Courselink but these are not intended to be stand-alone course notes. Some written lecture notes will be presented only in class. During lectures, the instructor will expand and explain the content of notes and provide example problems that supplement posted notes. Scheduled classes will be the principal venue to provide information and feedback for tests and labs.

8.2 Students' Learning Responsibilities

Students are expected to take advantage of the learning opportunities provided during lectures and lab sessions. Students, especially those having difficulty with the course content, should also make use of other resources recommended by the instructor. Students who do (or may) fall behind due to illness, work, or extra-curricular activities are advised to keep the instructor informed. This will allow the instructor to recommend extra resources in a timely

manner and/or provide consideration if appropriate.

8.3 Lab Safety

Safety is critically important to the School and is the responsibility of all members of the School: faculty, staff and students. As a student in a lab course you are responsible for taking all reasonable safety precautions and following the lab safety rules specific to the lab you are working in. In addition, you are responsible for reporting all safety issues to the laboratory supervisor, GTA or faculty responsible.

9 University Statements

9.1 Email Communication

As per university regulations, all students are required to check their e-mail account regularly: e-mail is the official route of communication between the University and its students.

9.2 When You Cannot Meet a Course Requirement

When you find yourself unable to meet an in-course requirement because of illness or compassionate reasons please advise the course instructor (or designated person, such as a teaching assistant) in writing, with your name, id#, and e-mail contact. The grounds for Academic Consideration are detailed in the Undergraduate and Graduate Calendars.

Undergraduate Calendar - Academic Consideration and Appeals
https://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-ac.shtml

Graduate Calendar - Grounds for Academic Consideration
https://www.uoguelph.ca/registrar/calendars/graduate/current/genreg/index.shtml

Associate Diploma Calendar - Academic Consideration, Appeals and Petitions
https://www.uoguelph.ca/registrar/calendars/diploma/current/index.shtml

9.3 Drop Date

Students will have until the last day of classes to drop courses without academic penalty. The deadline to drop two-semester courses will be the last day of classes in the second semester. This applies to all students (undergraduate, graduate and diploma) except for Doctor of Veterinary Medicine and Associate Diploma in Veterinary Technology (conventional and alternative delivery) students. The regulations and procedures for course registration are available in their respective Academic Calendars.

Undergraduate Calendar - Dropping Courses
https://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-drop.shtml

Graduate Calendar - Registration Changes
https://www.uoguelph.ca/registrar/calendars/graduate/current/genreg/genreg-reg-regchg.shtml

Associate Diploma Calendar - Dropping Courses
https://www.uoguelph.ca/registrar/calendars/diploma/current/c08/c08-drop.shtml

9.4 Copies of Out-of-class Assignments

Keep paper and/or other reliable back-up copies of all out-of-class assignments: you may be asked to resubmit work at any time.

9.5 Accessibility

The University promotes the full participation of students who experience disabilities in their academic programs. To that end, the provision of academic accommodation is a shared responsibility between the University and the student.

When accommodations are needed, the student is required to first register with Student Accessibility Services (SAS). Documentation to substantiate the existence of a disability is required; however, interim accommodations may be possible while that process is underway.

Accommodations are available for both permanent and temporary disabilities. It should be noted that common illnesses such as a cold or the flu do not constitute a disability.

Use of the SAS Exam Centre requires students to make a booking at least 14 days in advance, and no later than November 1 (fall), March 1 (winter) or July 1 (summer). Similarly, new or changed accommodations for online quizzes, tests and exams must be approved at least a week ahead of time.

For Guelph students, information can be found on the SAS website
https://www.uoguelph.ca/sas

For Ridgetown students, information can be found on the Ridgetown SAS website
https://www.ridgetownc.com/services/accessibilityservices.cfm

9.6 Academic Integrity

The University of Guelph is committed to upholding the highest standards of academic integrity, and it is the responsibility of all members of the University community-faculty, staff, and students-to be aware of what constitutes academic misconduct and to do as much as possible to prevent academic offences from occurring. University of Guelph students have the responsibility of abiding by the University's policy on academic misconduct regardless of their location of study; faculty, staff, and students have the responsibility of supporting an environment that encourages academic integrity. Students need to remain aware that instructors have access to and the right to use electronic and other means of detection.

Please note: Whether or not a student intended to commit academic misconduct is not relevant for a finding of guilt. Hurried or careless submission of assignments does not excuse students from responsibility for verifying the academic integrity of their work before submitting it. Students who are in any doubt as to whether an action on their part could be construed as an academic offence should consult with a faculty member or faculty advisor.

Undergraduate Calendar - Academic Misconduct
https://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-amisconduct.shtml

Graduate Calendar - Academic Misconduct
https://www.uoguelph.ca/registrar/calendars/graduate/current/genreg/index.shtml

9.7 Recording of Materials

Presentations that are made in relation to course work - including lectures - cannot be recorded or copied without the permission of the presenter, whether the instructor, a student, or guest lecturer. Material recorded with permission is restricted to use for that course unless further permission is granted.

9.8 Resources

The Academic Calendars are the source of information about the University of Guelph's procedures, policies, and regulations that apply to undergraduate, graduate, and diploma programs.

Academic Calendars
https://www.uoguelph.ca/academics/calendars

9.9 Illness

Medical notes will not normally be required for singular instances of academic consideration, although students may be required to provide supporting documentation for multiple missed assessments or when involving a large part of a course (e.g.. final exam or major assignment).
