ENGG*3380 Computer Organization and Design

01

Winter 2024
Section(s): 01

School of Engineering
Credit Weight: 0.50
Version 1.00 - January 05, 2024

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1 Course Details

1.1 Calendar Description

This course contains a detailed examination of modern computer organization and techniques for microprocessor architecture design. Topics include - CPU design; instruction set design, addressing modes, operands; data flow design: internal bus structure, data flow signals, registers; control sequence design: hardwired control, decoding, microprogramming; architecture classes: CISC, RISC, and DSP; Memory organization; performance. Students must complete a term project that includes design, implementation, and demonstration of a CPU using a hardware descriptive language like VHDL.

Pre-Requisites:	ENGG*2410
Restrictions:	This is a Priority Access Course. Enrolment may be restricted to the CENG specialization in the BENG and BENG:C programs. See department for more information. Non-BENG students may take a maximum of 4.00 ENGG credits.

1.2 Course Description

This course links several of the core courses in the Engineering Systems and Computing program (ENGG 2410, ENGG 3640, and CIS 3110) to provide a complete picture of how an electronics system that is composed of millions of transistors becomes a computing machine that can be used in a wide range of tasks. This course explore the hardware/software interface and study how modern computers are designed and evaluated.

1.3 Timetable

Lectures:

M/W/F 02:30PM - 03:20PM JTP, 2266

Laboratory:

Section 0101	Tue 01:30PM - 03:20PM RICH 1532
Section 0102	Mon 03:30PM - 05:20PM RICH 1532
Section 0103	Tue 08:30AM - 10:20AM RICH 1532
Section 0104	Wed 08:30AM - 10:20AM RICH 1532

1.4 Final Exam

Monday, April 22, 2024 08:30AM - 10:30AM Location TBA

Please see WebAdvisor for the latest information.

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2 Instructional Support

2.1 Instructional Support Team

Instructor: Mohamad Abou El Nasr Ph.D.
Email: mabouelnasr@uoguelph.ca
Office: THRN 1513
Office Hours: By appointment

Instructor: Haleh Vahedi
Email: hvahedi@uoguelph.ca
Telephone: +1-519-824-4120 x54741

2.2 Teaching Assistants

Teaching Assistant (GTA): Mohammad Dara
Email: dara@uoguelph.ca

Teaching Assistant (GTA): Erich MacLean
Email: emacle05@uoguelph.ca

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3 Learning Resources

3.1 Required Resources

Course Website (Website)
https://courselink.uoguelph.ca
Course material, news, announcements, and grades will be regularly posted to the ENGG*3380 Courselink site. You are responsible for checking the site regularly.

Computer Organization and Design: The hardware/software interface (Textbook)
A. Patterson and J.L. Hennessy, 6th Edition, Morgan Kaufmann.

3.2 Recommended Resources

VHDL for Engineers (Textbook)
Short, 2nd Edition, Prentice Hall, 2008.

Computer Organization and Architecture (Textbook)
Stallings, 11th Edition, Pearson.

Computer Systems Organization and Architecture (Textbook)
Carpinelli, Addison Wesley.

VHDL by Example: A Concise Introduction for FPGA Design (Textbook)
The same book is also available for Verilog under the name Verilog by Example: A Concise Introduction for FPGA Design

Computer Organization and Embedded Systems (Textbook)
Carl Hamacher and Zvonko Vranesic and Safwat Zaky and Naraig Manjikian., 6th Edition, McGraw Hill.

3.3 Additional Resources

Lecture Information (Notes)
All the lecture notes are posted on CourseLink

Lab Information (Lab Manual)
The handouts for all the lab sessions will be posted to CourseLink

Assignments (Notes)
assignments (if exist) will be posted to CourseLink and will be announced in lectures.

Miscellaneous Information (Other)
Other information related to Computer Organization are also posted on the webpage.

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4 Learning Outcomes

4.1 Course Learning Outcomes

By the end of this course, you should be able to:

1. Thoroughly understand computer organization and the impact of various components on performance
2. Evaluate computer performance
3. Design an instruction set to target a particular class of applications
4. Design a microprocessor including datapath and control unit
5. Implement a microprocessor design and measure its performance
6. Thoroughly understand microprocessor pipeline design and analyze its performance.
7. Understand memory hierarchy and design tradeoffs.
8. Thorough understanding of VHDL / Verilog and how it can be used to implement digital designs

4.2 Engineers Canada - Graduate Attributes (2018)

Successfully completing this course will contribute to the following:

#	Outcome	Learning Outcome
1	Knowledge Base	1, 2, 6, 8
1.1	Recall, describe and apply fundamental mathematical principles and concepts	2
1.3	Recall, describe and apply fundamental engineering principles and concepts	1, 2, 6
1.4	Recall, describe and apply program-specific engineering principles and concepts	1, 2, 6, 8
2	Problem Analysis	2, 4
2.1	Formulate a problem statement in engineering and non-engineering terminology	4
2.2	Identify, organize and justify appropriate information, including assumptions	2, 4
2.3	Construct a conceptual framework and select an appropriate solution approach	4
2.4	Execute an engineering solution	4
2.5	Critique and appraise solution approach and results	4
3	Investigation	3, 4
3.2	Design and apply an experimental plan/investigative approach (for example, to characterize, test or troubleshoot a system)	3, 4

#	Outcome	Learning Outcome
3.3	Analyze and interpret experimental data	3, 4
4	Design	3, 4, 5, 7
4.1	Describe design process used to develop design solution	3, 4, 7
4.2	Construct design-specific problem statements including the definition of criteria and constraints	3, 4, 7
4.3	Create a variety of engineering design solutions	3, 4, 7
4.4	Evaluate alternative design solutions based on problem definition	3, 4, 7
4.5	Develop and refine an engineering design solution, through techniques such as iteration, simulation and/or prototyping	3, 4, 5, 7
5	Use of Engineering Tools	3, 4, 5, 8
5.1	Select appropriate engineering tools from various alternatives	3, 4
5.2	Demonstrate proficiency in the application of selected engineering tools	3, 4, 5, 8
5.3	Recognize limitations of selected engineering tools	3, 4, 8
6	Individual & Teamwork	3, 4
6.1	Describe principles of team dynamics and leadership	3, 4
6.2	Understand all members’ roles and responsibilities within a team	3, 4
6.3	Execute and adapt individual role to promote team success through, for example, timeliness, respect, positive attitude	3, 4
6.4	Apply strategies to mitigate and/or resolve conflicts	3, 4
6.5	Demonstrate leadership through, for example, influencing team vision and process, promoting a positive team culture, and inspiring team members to excel	3, 4
7	Communication Skills	7
7.2	Interpret technical documentation such as device specification sheets, drawings, diagrams, flowcharts, and pseudocode	7
7.3	Construct the finished elements using accepted norms in English, graphical standards, and engineering conventions, as appropriate for the message and audience	7

4.3 Relationships with other Courses

Previous Courses:

ENGG*2410: Principles of digital computing systems, introduction to VHDL

Follow-up Courses:

ENGG*3640 Microcomputer Interfacing: Interfacing computer to external equipment and data acqui- sition systems.

ENGG*4540 Advanced Computer Architecture: extend the architecture topics covered in ENGG 3380 to more advanced areas like instruction level parallelism and multi-core processors.

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5 Teaching and Learning Activities

5.1 Lecture

Topics:	Introduction to computers and Performance Issues (~1 Week)
References:	Patterson (Ch.1)
Learning Outcome:	1, 2
Topics:	Instruction Set Architecture (~2 Weeks)
References:	Patterson(Ch.2)
Learning Outcome:	3
Topics:	Arithmetic for Computers (~1 Weeks)
References:	Patterson (Ch.3)
Learning Outcome:	4
Topics:	CPU Design, Data Path (~ 2 Weeks)

References: Patterson (Ch.4)

Learning Outcome: 4

Topics: CPU Design, Control (MicroProg) (~2Weeks)

References: Patterson(D-2)

Learning Outcome: 3, 4

Topics: Pipelining (~1 Week)

References: Patterson (Ch.4)

Learning Outcome: 6

Topics: Memory hierarchy (Cache) (~ 2 Weeks)

References: Patterson (Ch.5)

Learning Outcome: 7

Topics: Review

5.2 Lab

Week 2

Topics: The labs in this course are designed to cover VHDL / Verilog design and simulation of Single Cycle and pipelined CPU. The labs cover the VHDL and the FPGA board used to implement the project design. Additional information regarding the labs will be posted on the web page.

L1: Intro to Vivado, (VHDL / Verilog) circuit design and simulation, ModelSim

(Time Multiplexed 7-segment Display).

Learning Outcome: 1
Demo: Yes
Report: None

Week 3

Topics: MARS Simulator

Learning Outcome: 1, 2
Demo: Yes
Report: Yes

Week 4

Topics: L2: Implementing Register Files & Memory in VHDL / Verilog.

Learning Outcome: 7, 8
Demo: Yes
Report: Yes

Week 5

Topics: ALU Design

Learning Outcome: 1
Demo: Yes
Report: Yes

Week 6

Topics: hardwired / Micro Programmed Control Units

Learning Outcome: 4, 5
Demo: Yes
Report: Yes

Week 7

Topics: Single Cycle MIPS Processor

Integration: ALU + RegFile + Memory + Control Unit

Learning Outcome: 5, 8
Demo: Yes
Report: Yes

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6 Assessments

6.1 Marking Schemes & Distributions

There will be no make up for the midterms. If you miss a midterm due to grounds for granting academic consideration or religious accommodation, the weight of the missed midterm will be added to the final exam.

Name	Scheme A (%)
Assignments	0
Labs	20
Midterm	25
Project	20
Final	35
Total	100

6.2 Assessment Details

Assignment (0%)
Learning Outcome: 1, 2, 3, 4, 5, 6, 7, 8
Assignments will not be graded however solving them is crucial, assignment problems are your best practice for midterm and final.

Labs (20%)
Date: Due dates
Learning Outcome: 1, 2, 3, 4, 5, 6, 7, 8
Labs reports and/or Demos are due one week after they are given or as indicated in the lab handouts and posted on Courselink.

Late submissions of lab reports will be subject to the following penalty policy.

- 25% will be deducted if the report is up to 24 hours late,
- 50% will be deducted if the report is 24 to 48 hours late,
- No reports will be accepted after 48 hours of the due date.

While the labs are expected to be carried in a face to face fashion, if unforeseen situation prevents such a delivery method, we will rely on MARS and VIVADO simulations and online demos.

Project (20%)
Learning Outcome: 1, 2, 3, 4, 5, 6, 7, 8
Project phase 1 Report: Week 8 (25%)

Project phase 2 Report; Week 10 (30%)

Final Report and Demo: Week 12 (45%)

Midterm Exams (25%)
Date: Week 7, Lectures
Learning Outcome: 1, 2, 6, 7
Midterm will be closed book and will cover all materials introduced in lectures and labs. Details, specific date and time will be announced on course link. If there are any modifications, they will be given in lectures and announced on courselink.

Final Exam (35%)
Date: Mon, Apr 24, 08:30 AM - , 9:00 PM, (Location TBA)
Learning Outcome: 1, 2, 6, 7

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7 Course Statements

7.1 Course Grading Policies

Missed Assessments: If you are unable to meet an in-course requirement due to medical, psychological, or compassionate reasons, please email the course instructor. See the undergraduate calendar for information on regulations and procedures for Academic Consideration: http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-ac.shtml

Accommodation of Religious Obligations: If you are unable to meet an in-course requirement due to religious obligations, please email the course instructor within two weeks of the start of the assessment to make alternate arrangements. See the undergraduate calendar for information on regulations and procedures for Academic Consideration of Religious Obligations: http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-accomrelig.shtml

Passing grade: In order to pass the course, you must pass both the laboratory and exam portions. Students must obtain a grade of 50% or higher on the exam portion of the course in order for the laboratory write-up portion of the course to count towards the final grade.

Missed midterm: If you miss a test due to grounds for granting academic consideration or religious accommodation, the weight of any missed test will be added to the final exam weight. There will be **no makeup midterm tests**.

Lab Work: You must attend and complete all laboratories. If you miss a laboratory due to grounds for granting academic consideration or religious accommodation, arrangements must be made with the teaching assistant to complete a makeup lab.

Late Lab Reports: Late submissions of lab reports will be subject to the following penalty policy.

- 25% will be deducted if the report is up to 24 hours late,

- 50% will be deducted if the report is 24 to 48 hours late,
- No reports will be accepted after 48 hours of the due date.

8 School of Engineering Statements

8.1 Instructor's Role and Responsibility to Students

The instructor’s role is to develop and deliver course material in ways that facilitate learning for a variety of students. Selected lecture notes will be made available to students on Courselink but these are not intended to be stand-alone course notes. Some written lecture notes will be presented only in class. During lectures, the instructor will expand and explain the content of notes and provide example problems that supplement posted notes. Scheduled classes will be the principal venue to provide information and feedback for tests and labs.

8.2 Students' Learning Responsibilities

Students are expected to take advantage of the learning opportunities provided during lectures and lab sessions. Students, especially those having difficulty with the course content, should also make use of other resources recommended by the instructor. Students who do (or may) fall behind due to illness, work, or extra-curricular activities are advised to keep the instructor informed. This will allow the instructor to recommend extra resources in a timely manner and/or provide consideration if appropriate.

8.3 Lab Safety

Safety is critically important to the School and is the responsibility of all members of the School: faculty, staff and students. As a student in a lab course you are responsible for taking all reasonable safety precautions and following the lab safety rules specific to the lab you are working in. In addition, you are responsible for reporting all safety issues to the laboratory supervisor, GTA or faculty responsible.

9 University Statements

9.1 Email Communication

As per university regulations, all students are required to check their e-mail account regularly: e-mail is the official route of communication between the University and its students.

9.2 When You Cannot Meet a Course Requirement

When you find yourself unable to meet an in-course requirement because of illness or compassionate reasons please advise the course instructor (or designated person, such as a teaching assistant) in writing, with your name, id#, and e-mail contact. The grounds for Academic Consideration are detailed in the Undergraduate and Graduate Calendars.

Undergraduate Calendar - Academic Consideration and Appeals
https://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-ac.shtml

Graduate Calendar - Grounds for Academic Consideration
https://www.uoguelph.ca/registrar/calendars/graduate/current/genreg/index.shtml

Associate Diploma Calendar - Academic Consideration, Appeals and Petitions
https://www.uoguelph.ca/registrar/calendars/diploma/current/index.shtml

9.3 Drop Date

Students will have until the last day of classes to drop courses without academic penalty. The deadline to drop two-semester courses will be the last day of classes in the second semester. This applies to all students (undergraduate, graduate and diploma) except for Doctor of Veterinary Medicine and Associate Diploma in Veterinary Technology (conventional and alternative delivery) students. The regulations and procedures for course registration are available in their respective Academic Calendars.

Undergraduate Calendar - Dropping Courses
https://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-drop.shtml

Graduate Calendar - Registration Changes
https://www.uoguelph.ca/registrar/calendars/graduate/current/genreg/genreg-reg-regchg.shtml

Associate Diploma Calendar - Dropping Courses
https://www.uoguelph.ca/registrar/calendars/diploma/current/c08/c08-drop.shtml

9.4 Copies of Out-of-class Assignments

Keep paper and/or other reliable back-up copies of all out-of-class assignments: you may be asked to resubmit work at any time.

9.5 Accessibility

The University promotes the full participation of students who experience disabilities in their academic programs. To that end, the provision of academic accommodation is a shared responsibility between the University and the student.

When accommodations are needed, the student is required to first register with Student Accessibility Services (SAS). Documentation to substantiate the existence of a disability is required; however, interim accommodations may be possible while that process is underway.

Accommodations are available for both permanent and temporary disabilities. It should be noted that common illnesses such as a cold or the flu do not constitute a disability.

Use of the SAS Exam Centre requires students to make a booking at least 14 days in advance, and no later than November 1 (fall), March 1 (winter) or July 1 (summer). Similarly, new or changed accommodations for online quizzes, tests and exams must be approved at least a week ahead of time.

For Guelph students, information can be found on the SAS website
https://www.uoguelph.ca/sas

For Ridgetown students, information can be found on the Ridgetown SAS website
https://www.ridgetownc.com/services/accessibilityservices.cfm

9.6 Academic Integrity

The University of Guelph is committed to upholding the highest standards of academic integrity, and it is the responsibility of all members of the University community-faculty, staff, and students-to be aware of what constitutes academic misconduct and to do as much as possible to prevent academic offences from occurring. University of Guelph students have the responsibility of abiding by the University's policy on academic misconduct regardless of their location of study; faculty, staff, and students have the responsibility of supporting an environment that encourages academic integrity. Students need to remain aware that instructors have access to and the right to use electronic and other means of detection.

Please note: Whether or not a student intended to commit academic misconduct is not relevant for a finding of guilt. Hurried or careless submission of assignments does not excuse students from responsibility for verifying the academic integrity of their work before submitting it. Students who are in any doubt as to whether an action on their part could be construed as an academic offence should consult with a faculty member or faculty advisor.

Undergraduate Calendar - Academic Misconduct
https://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-amisconduct.shtml

Graduate Calendar - Academic Misconduct
https://www.uoguelph.ca/registrar/calendars/graduate/current/genreg/index.shtml

9.7 Recording of Materials

Presentations that are made in relation to course work - including lectures - cannot be recorded or copied without the permission of the presenter, whether the instructor, a student, or guest lecturer. Material recorded with permission is restricted to use for that course unless further permission is granted.

9.8 Resources

The Academic Calendars are the source of information about the University of Guelph's procedures, policies, and regulations that apply to undergraduate, graduate, and diploma programs.

Academic Calendars
https://www.uoguelph.ca/academics/calendars

9.9 Illness

Medical notes will not normally be required for singular instances of academic consideration, although students may be required to provide supporting documentation for multiple missed assessments or when involving a large part of a course (e.g.. final exam or major assignment).
