



# ENGG\*2410 Digital Systems Design Using Descriptive Languages

01

Fall 2023

Section(s): C01

School of Engineering

Credit Weight: 0.50

Version 1.00 - September 07, 2023

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## 1 Course Details

### 1.1 Calendar Description

Review of Boolean algebra and truth tables, Karnaugh maps. Design, synthesis and realization of combinational circuits. Design, synthesis and realization of sequential circuits. VHDL: structural modeling, data flow modeling, synchronous & asynchronous behavior descriptions, algorithmic modeling. Designing with PLDs. Digital design with SM charts. Designing with PGAs and complex programmable logical devices. Hardware testing and design for testability. Hierarchy in large designs. The course will primarily be concerned with the design of multi-input, multi-output digital controllers which provide the central control signals that orchestrate the collection of hardware devices (from SSI to VLSI) found in a digital system. An introduction to FPGA-based, as well as microprocessor-based digital systems design will be given. Design examples will include systems such as UART, microcontroller CPU, ALU and data acquisition system.

**Pre-Requisites:**

PHYS\*1130, (1 of CIS\*1300, CIS\*1500, ENGG\*1410)

**Restrictions:**

This is a Priority Access Course. Enrolment may be restricted to the CENG and ESC specializations in the BENG and BENG:C programs. See department for more information. Non-BENG students may take a maximum of 4.00 ENGG credits.

### 1.2 Course Description

This course is an introductory course in digital logic design, which is a basic course in most electrical and computer engineering programs. The main goals of the course are (1) to teach students the fundamental concepts in classical manual digital design and (2) to illustrate clearly the way in which digital circuits are designed today, using CAD tools.

## 1.3 Timetable

### Lectures:

- Tuesday 11:30 AM - 12:50 PM, ALEX 100, Shawki Areibi
- Thursday 11:30 AM - 12:50 PM, ALEX 100, Shawki Areibi

### Seminars (Tutorials):

- Monday, Time: 10:30 AM - 11:20 AM, Location: MINS 017, GTA: Meghan Yesji
- Tuesday, Time: 10:30 AM - 11:20 AM, Location: MCKN 234, GTA: Erich MacLean
- Wednesday, Time: 8:30 AM - 9:20 AM, Location: MINS 017, GTA: Vibhuti Bajaj
- Thursday, Time: 10:30 AM - 11:20 AM, Location: MINS 017, GTA: Dixit Patel

### Laboratory:

- Monday, Time: 8:30 AM - 10:20 AM, Location: RICH 1532, GTA: Erich MacLean, emacle05@uoguelph.ca
- Tuesday, Time: 8:30 AM - 10:20 AM, Location: RICH 1532, GTA: Dixit Patel, dixitpiy@uoguelph.ca
- Thursday, Time: 8:30 AM - 10:20 AM, Location: RICH 1532, GTA: Vibhuti Bajaj, vbajaj@uoguelph.ca
- Friday, Time: 8:30 AM - 10:20 AM, Location: RICH 1532, GTA: Meghan Yesji, myesji@uoguelph.ca

## 1.4 Final Exam

December 12th 2023, 11:30 AM, (Location, TBA)

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## 2 Instructional Support

### 2.1 Instructional Support Team

<b>Instructor:</b>	Shawki Areibi
<b>Email:</b>	sareibi@uoguelph.ca
<b>Telephone:</b>	5198244120 x53819
<b>Office:</b>	Thornbrough Building SOE 2335
<b>Office Hours:</b>	by appointment

## 2.2 Lab Instructor

Haleh Vahedi

Office: RICH 1509

Telephone: x54741

Email: hvahedi@uoguelph.ca

## 2.3 Teaching Assistants

### Teaching Assistant #1:

Erich MacLean, Office: THRN 1425, Email: emacle05@uoguelph.ca, office hours: Monday, 13:00 - 14:00 PM

### Teaching Assistant #2:

Dixit Pi Patel, Office: THRN 1425, Email: dixitpiy@uoguelph.ca, office hours: Thursday, 13:00 - 14:00 PM

### Teaching Assistant #3

Meghan Durwas Yesji, Office: THRN 1425, Email: myesji@uoguelph.ca, office hours: Wednesday, 13:00 - 14:00 PM

### Teaching Assistant #4:

Vibhuti Hariom Bajaj, office: THRN 1425, Email: vbajaj@uoguelph.ca, office hours: Tuesday, 15:00 - 16:00 PM

### Teaching Assistant #5:

Mohammad Dara, office: Thorn Bldg. Email: dara@uoguelph.ca, office hours: by appointment

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## 3 Learning Resources

### 3.1 Required Resources

#### CourseLink (Website)

Course material, news, announcements, and grades will be regularly posted to the

ENGG\*2410 CourseLink. You are responsible for checking the site regularly.

**M. Morris Mano Logic And Computer Design Fundamentals, forth Edition, Pearson, 2014 (Textbook)**

## 3.2 Recommended Resources

**VHDL for Engineers (Textbook)**

K. Short, 2nd Edition, Prentice Hall, 2008.

**VHDL Tutorial by Shawki Areibi (Article)**

## 3.3 Additional Resources

**Lecture Information (Notes)**

All the lecture notes will be posted on CourseLink

**Lab Information (Notes)**

The handouts for all the lab sessions will be posted on CourseLink.

**Assignments (Other)**

The assignments will be posted on CourseLink.

**Miscellaneous Information (Other)**

Other information related to Digital Design are also posted on the web page.

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# 4 Learning Outcomes

## 4.1 Course Learning Outcomes

By the end of this course, you should be able to:

1. Understand basic digital concepts and combinational digital logic.
2. Design and Analysis of basic/advanced combinational digital circuits.
3. Design and Analysis of basic/advanced sequential digital circuits.
4. Implement Finite State Machines and designing control units.
5. Ability to build combinational logic circuits out of standard TTL/CMOS parts.
6. Ability to use FPGAs and modern CAD tools for logic design.

## 4.2 Engineers Canada - Graduate Attributes (2018)

Successfully completing this course will contribute to the following:

#	Outcome	Learning Outcome
1	Knowledge Base	1, 2, 4, 5
1.3	Recall, describe and apply fundamental engineering principles and concepts	1, 2, 4, 5
1.4	Recall, describe and apply program-specific engineering principles and concepts	1
2	Problem Analysis	2, 3
2.2	Identify, organize and justify appropriate information, including assumptions	2, 3
4	Design	2, 3, 4, 5
4.1	Describe design process used to develop design solution	2, 3, 4, 5
4.2	Construct design-specific problem statements including the definition of criteria and constraints	2
5	Use of Engineering Tools	2, 3, 4, 5, 6
5.1	Select appropriate engineering tools from various alternatives	2, 3, 4, 6
5.2	Demonstrate proficiency in the application of selected engineering tools	5
6	Individual & Teamwork	3, 4
6.1	Describe principles of team dynamics and leadership	4
6.2	Understand all members' roles and responsibilities within a team	3
7	Communication Skills	1
7.1	Identify key message(s) and intended audience in verbal or written communication as both sender and receiver	1

## 5 Teaching and Learning Activities

### 5.1 Lecture

<b>Topics:</b>	Introduction to Digital Systems
<b>References:</b>	Chapter 1
<b>Topics:</b>	Combinational Logic Circuits
<b>References:</b>	Chapter 2

<b>Topics:</b>	Combinational Logic Analysis
<b>References:</b>	Chapter 3
<b>Topics:</b>	Combinational Logic Design (VHDL)
<b>References:</b>	Chapter 3,4
<b>Topics:</b>	Arithmetic Circuits (VHDL)
<b>References:</b>	Chapter 4
<b>Topics:</b>	Basic Sequential Circuits (Analysis)
<b>References:</b>	Chapter 5
<b>Topics:</b>	Sequential Circuit Design (VHDL)
<b>References:</b>	Chapter 5
<b>Topics:</b>	Registers and Counters (VHDL)
<b>References:</b>	Chapter 7
<b>Topics:</b>	RTL Register Transfer and Data Path
<b>References:</b>	Chapter 7
<b>Topics:</b>	Design of Control Units and ASMs
<b>References:</b>	Chapter 7
<b>Topics:</b>	Memory (SRAM, DRAM)
<b>References:</b>	Chapter 8
<b>Topics:</b>	Programmable Logic Devices
<b>References:</b>	Chapter 10

## 5.2 Lab

### Week 1

<b>Topics:</b>	L0: Intro to Lab Equipment and Safety Training
Report:	None
Due:	---

### Week 2

<b>Topics:</b>	L1: Tutorial, Xilinx CAD Flow, Schematic Capture
Duration:	2 Weeks
Report:	Yes
Due:	Week #4 in Drop Box

**Week 4**

**Topics:** L2: Combinational Logic Design (Trip Genie), Schematic Capture

Duration: 2 Weeks

Report: Yes

Due: Week #6 in Drop Box

**Week 6**

**Topics:** L3: Tutorial, Xilinx CAD Flow, VHDL

Duration: 1 Week

Report: Yes

Due: Week #7 in Drop Box

**Week 7**

**Topics:** L4: Design of Decoders and 7-Segment Display

Duration: 1 Week

Report: Yes

Due: Week #8 in Drop Box

**Week 8**

**Topics:** L5: Arithmetic Circuits ``Adder/Subtractor", VHDL

Duration: 1 Week

Report: Yes

Due: Week #9 in Drop Box

**Week 9**

**Topics:** L6: Sequential Logic Design (Sequence Recognizer), VHDL

Duration: 1 Week

Report: Yes

Due: Week #10 in Drop Box

**Week 10****Topics:** L7: Data Path Design (Arithmetic Logic Units), VHDL

Duration: 2 Weeks

Report: Yes

Due: Week 12 in Drop Box

**5.3 Other Important Dates****Thursday, 7th September 2023:** Classes Start.**Monday, 9th October 2023:** Thanks Giving Holiday.**Tuesday, 10th October 2023:** Fall Study Break, No Classes Scheduled.**Thursday, 30th November 2023:** Lecture (Tuesday Oct. 10th Schedule in Effect).**Friday, 1st December 2023:** Last Class (Monday Oct 9th Schedule in Effect).**6 Assessments****6.1 Marking Schemes & Distributions**

**Missed Assessments:** If you are unable to meet an in-course requirement due to medical, psychological, or compassionate reasons, please email the course instructor. See the undergraduate calendar for information on regulations and procedures for Academic Consideration:

<http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-ac.shtml>

**Accommodation of Religious Obligations:** If you are unable to meet an in-course requirement due to religious obligations, please email the course instructor within two weeks of the start of the semester to make alternate arrangements. See the undergraduate calendar for information on regulations and procedures for Academic Consideration of Religious Obligations:

<http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-accomrelig.shtml>

**Passing grade:** The passing grade in this course is 50%. Students must obtain a grade of 45% or higher on the exam portion of the course in order for the laboratory write-up portion of the course to count towards the final grade.

**Missed midterm/quiz tests:** If you miss a test due to grounds for granting academic consideration or religious accommodation, the weight of any missed test will be added to the final exam weight. There will be no makeup midterm/quizzes tests.

**Lab Work:** You must attend and complete all laboratories. If you miss a laboratory due to grounds for granting academic consideration or religious accommodation, arrangements must be made with the teaching assistant to complete a makeup lab.



**Late Lab Reports:** Late submissions of lab reports will be penalized unless you have good reasons. Explain to your teaching assistant the circumstances of why your lab report is submitted late.

Name	Scheme A (%)
Assignments	5
Labs	20
Midterm	30
Final Exam	45
Total	100

## 6.2 Assessment Details

### Assignments (5%)

**Learning Outcome:** 1, 2, 4

There will be 10 assignments throughout the term. Solve all problems and hand in your assignment to the teaching assistant in the tutorial.

### Labs (20%)

**Learning Outcome:** 1, 2, 3, 4, 5, 6

There will be 7 labs throughout the term.

### Midterm Exam (30%)

**Date:** Week 7

### Final Exam (45%)

**Date:** Tue, Dec 12, 11:30 AM - 1:30 PM, TBA

**Learning Outcome:** 1, 2, 3, 4, 5

## 7 School of Engineering Statements

### 7.1 Instructor's Role and Responsibility to Students

The instructor's role is to develop and deliver course material in ways that facilitate learning for a variety of students. Selected lecture notes will be made available to students on Courselink but these are not intended to be stand-alone course notes. Some written lecture notes will be presented only in class. During lectures, the instructor will expand and explain the content of notes and provide example problems that supplement posted notes. Scheduled classes will be the principal venue to provide information and feedback for tests and labs.

### 7.2 Students' Learning Responsibilities

Students are expected to take advantage of the learning opportunities provided during lectures and lab sessions. Students, especially those having difficulty with the course content, should also make use of other resources recommended by the instructor. Students who do (or may) fall behind due to illness, work, or extra-curricular activities are advised to keep the instructor informed. This will allow the instructor to recommend extra resources in a timely manner and/or provide consideration if appropriate.

### **7.3 Lab Safety**

Safety is critically important to the School and is the responsibility of all members of the School: faculty, staff and students. As a student in a lab course you are responsible for taking all reasonable safety precautions and following the lab safety rules specific to the lab you are working in. In addition, you are responsible for reporting all safety issues to the laboratory supervisor, GTA or faculty responsible.

## **8 University Statements**

### **8.1 Email Communication**

As per university regulations, all students are required to check their e-mail account regularly: e-mail is the official route of communication between the University and its students.

### **8.2 When You Cannot Meet a Course Requirement**

When you find yourself unable to meet an in-course requirement because of illness or compassionate reasons please advise the course instructor (or designated person, such as a teaching assistant) in writing, with your name, id#, and e-mail contact. The grounds for Academic Consideration are detailed in the Undergraduate and Graduate Calendars.

Undergraduate Calendar - Academic Consideration and Appeals

<https://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-ac.shtml>

Graduate Calendar - Grounds for Academic Consideration

<https://www.uoguelph.ca/registrar/calendars/graduate/current/genreg/index.shtml>

Associate Diploma Calendar - Academic Consideration, Appeals and Petitions

<https://www.uoguelph.ca/registrar/calendars/diploma/current/index.shtml>

### **8.3 Drop Date**

Students will have until the last day of classes to drop courses without academic penalty. The deadline to drop two-semester courses will be the last day of classes in the second semester. This applies to all students (undergraduate, graduate and diploma) except for Doctor of Veterinary Medicine and Associate Diploma in Veterinary Technology (conventional and alternative delivery) students. The regulations and procedures for course registration are available in their respective Academic Calendars.

Undergraduate Calendar - Dropping Courses

<https://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-drop.shtml>

Graduate Calendar - Registration Changes

<https://www.uoguelph.ca/registrar/calendars/graduate/current/genreg/genreg-reg-regchg.shtml>

Associate Diploma Calendar - Dropping Courses

<https://www.uoguelph.ca/registrar/calendars/diploma/current/c08/c08-drop.shtml>

## 8.4 Copies of Out-of-class Assignments

Keep paper and/or other reliable back-up copies of all out-of-class assignments: you may be asked to resubmit work at any time.

## 8.5 Accessibility

The University promotes the full participation of students who experience disabilities in their academic programs. To that end, the provision of academic accommodation is a shared responsibility between the University and the student.

When accommodations are needed, the student is required to first register with Student Accessibility Services (SAS). Documentation to substantiate the existence of a disability is required; however, interim accommodations may be possible while that process is underway.

Accommodations are available for both permanent and temporary disabilities. It should be noted that common illnesses such as a cold or the flu do not constitute a disability.

Use of the SAS Exam Centre requires students to make a booking at least 14 days in advance, and no later than November 1 (fall), March 1 (winter) or July 1 (summer). Similarly, new or changed accommodations for online quizzes, tests and exams must be approved at least a week ahead of time.

For Guelph students, information can be found on the SAS website

<https://www.uoguelph.ca/sas>

For Ridgetown students, information can be found on the Ridgetown SAS website

<https://www.ridgetownc.com/services/accessibilityservices.cfm>

## 8.6 Academic Integrity

The University of Guelph is committed to upholding the highest standards of academic integrity, and it is the responsibility of all members of the University community—faculty, staff, and students—to be aware of what constitutes academic misconduct and to do as much as possible to prevent academic offences from occurring. University of Guelph students have the responsibility of abiding by the University's policy on academic misconduct regardless of their location of study; faculty, staff, and students have the responsibility of supporting an environment that encourages academic integrity. Students need to remain aware that instructors have access to and the right to use electronic and other means of detection.

Please note: Whether or not a student intended to commit academic misconduct is not

relevant for a finding of guilt. Hurried or careless submission of assignments does not excuse students from responsibility for verifying the academic integrity of their work before submitting it. Students who are in any doubt as to whether an action on their part could be construed as an academic offence should consult with a faculty member or faculty advisor.

Undergraduate Calendar - Academic Misconduct

<https://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-amisconduct.shtml>

Graduate Calendar - Academic Misconduct

<https://www.uoguelph.ca/registrar/calendars/graduate/current/genreg/index.shtml>

## **8.7 Recording of Materials**

Presentations that are made in relation to course work - including lectures - cannot be recorded or copied without the permission of the presenter, whether the instructor, a student, or guest lecturer. Material recorded with permission is restricted to use for that course unless further permission is granted.

## **8.8 Resources**

The Academic Calendars are the source of information about the University of Guelph's procedures, policies, and regulations that apply to undergraduate, graduate, and diploma programs.

Academic Calendars

<https://www.uoguelph.ca/academics/calendars>

## **8.9 Illness**

Medical notes will not normally be required for singular instances of academic consideration, although students may be required to provide supporting documentation for multiple missed assessments or when involving a large part of a course (e.g.. final exam or major assignment).

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