ENGG 3380 Computer Organization and Design

Fall 2010

What is this course about?

This course provides detailed examination of modern computer organization and techniques for microprocessor architecture design. Topics include - CPU design; instruction set design, addressing modes, operands; data flow design: internal bus structure, data flow signals, registers; control sequence design: hardwired control, decoding, microprogramming; architecture classes: CISC, RISC, and DSP; Memory organization; performance. Students must complete a term project that includes design, implementation, and demonstration of a CPU using a hardware descriptive language like VHDL

Why take this course?

This course links several of the core courses in the Engineering Systems and Computing program (ENGG 2410, ENGG 3640, and CIS 3110) to provide a complete picture of how an electronics system that is composed of millions of transistors becomes a computing machine that can be used in a wide range of tasks. This course explore the hardware/software interface and study how modern computers are designed and evaluated.

Learning objectives

BY the end of this course, students should be able to

⇒ Thoroughly understand computer organization and the impact of various components on performance.

⇒ Evaluate computer performance

⇒ Design an instruction set to target a particular class of applications

⇒ Design a microprocessor including datapath and control unit

⇒ Analyze pipelining designs.

⇒ Analyze memory management designs.

Who is teaching this course?

⇒ **Instructor** Dr. Medhat Moussa

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Office Hours: By appointment

⇒ **Teaching Assistant** Antony Savich, asavich@uoguelph.ca

How is it delivered?

The course will be delivered through 3 lectures and 2 hours lab/week.

Lectures: MACH 308 MWF 10:30AM - 11:20AM

Lab.: THRN 2307 TH 12:30 PM - 2:20 PM

Final Exam: Dec 8, 2010, 19:00 -21:00h, location TBD

Course website: http://courselink.uoguelph.ca/

⇒ **Textbooks:**

1. D. A. Patterson and J.L. Hennessy, *Computer Organization and Design: The hardware/software interface*, 3nd ed. Morgan Kaufmann. (Main textbook)

Lectures will also include materials covered in the following texts for microprocessor design and implementation.

1. J.L. Hennessy and D. A. Patterson, *Computer Architecture: A Quantitative Approach*, 4th ed., Morgan Kaufmann
2. C. Hamacher, Z. Vranesic, S. Zaky, *Computer Organization*, 5*th* edition, McGraw Hill.
3. J. Carpinelli, *Computer Systems Organization and Architecture*, Addison Wesley.
4. W. Stallings, *Computer Organization and Architecture*. 5*th* edition, Prentice Hall
5. Morris Mano and C. Kime, *Logic And Computer Design Fundamentals,* 2nd Ed., Prentice Hall.

How to get feedback and how is your work is evaluated?

The course applies a design-centric approach to teaching computer organization and design. Students are required to complete a term long project that focuses on designing, implementing, and testing a simple microprocessor. Labs will help build students expertise in VHDL and how it can be used in implementation of digital designs on FPGAs. This will make it easy to implement and test the student design within the time allocated to finish the project. The total mark of the course is divided as follows:

⇒ Project 45% (divided over several phases)

⇒ Lab report and assignments 15%

⇒ Final Exam 40%

Outline

Review of Technology Trends and Cost/Performance (Patterson, Ch4)	Week 1
Review of Technology Trends and Cost/Performance, Processor Performance Trends, The Task of a Computer Designer, Definition of Computer Architecture, Cost/Performance Analysis, Fundamental “Laws”/Principles, SPEC: System Performance Evaluation Cooperative, Amdal's Law	
Instruction Set Architecture (Patterson, Ch2)	Week 2-3
Introduction to MIPS ISA(Outside source), Alternative Architectures and ISA design factors, ISA and Machine Format Design	
CPU Design, Datapath (Hamacher, Ch9; Carpinelli, Ch6)	Week 4
Datapath Components, Register transfer Language, Complete instruction execution, Branch instruction, Multiple-Bus Organization	
CPU Design, Control (Hamacher, Ch9)	Week 5-6
Hardwired Control, Microprogramming Control	
Pipelining (Patterson,, Ch6)	Week 7-11
Pipeline Registers, Pipelining Hazards, Stalls, Structural hazards, Data hazards, Control Hazards, Control Implementation for Data Hazards, Delayed branches,Loop unrolling, Dependency, Data Dependency, Name Dependency, Control Dependency	
Memory hierarchy (Patterson,, Ch7)	Week 12