ENGG*2410: Digital Systems Design
School of Engineering
University of Guelph
Fall 2011

Course Outline

Prerequisites: PHY1130, CIS1500

Instructor

Prof:	Antony Savich
Office:	THRN 1415
Phone:	(519) 824-4120 x53644
Email:	asavich@uoguelph.ca
Web Site:	http://courselink.uoguelph.ca/
Office Hours:	Mondays 14:30 - 15:30 or by appointment

Lab Coordinator & Teaching Assistant

Lab Coordinator	TAs	
Nate Groendyk	Ahmed Alwattar	Omar Ahmed
THRN 2308, x53873	THRN 2319	THRN 2319
groendyk@uoguelph.ca	aalwatta@uoguelph.ca	oahmed@uoguelph.ca

Lecture & Lab Schedule

	Day	Section	Time	Place
Lectures	Mon	11/12/21/22	15:30 - 16:20	MACK 031
	Wed	11/12/21/22	15:30 - 16:20	MACK 031
	Fri	11/12/21/22	15:30 - 16:20	MACK 031
Tutorials	Mon	11/21	16:30-17:20	MACK 228
	Wed	12/22	16:30-17:20	MACK 227
Labs	Tue	11/12	12:30-14:20	THRN 2307
	Thu	21/22	12:30-14:20	THRN 2307

Course Text

1. M. Morris Mano *Logic And Computer Design Fundamentals 4th Edition* Prentice Hall, 2008

References

1. K. Short, *VHDL for Engineers*, 2nd Edition, Prentice Hall, 2008.
2. S. Yalamanchili, *VHDL, A Starter's Guide*, 2nd Edition, Prentice Hall, 2005.
3. VHDL Tutorial by Shawki Areibi.
4. Tutorial On Using Xilinx Foundation Design Tools.
5. Fundamentals of Digital Logic with VHDL Design by Brown and Vranesic.

Course Contents, Goals and Objectives:

Digital hardware plays a prominent role in many electrical and computer engineering products today. This is principally due to the rapid increase in transistor densities and speed of integrated circuits and steep decline in their cost caused by the advance in micro-electronic implementation technologies. This trend is likely to continue in the foreseeable future.

This course is an introductory course in digital logic design, which is a basic course in most computer, electrical and mechanical engineering programs. The main goals of the course are (1) to teach students the fundamental concepts in classical manual digital design and (2) to illustrate clearly the way in which digital circuits are designed today, using CAD tools. Throughout the course basic concepts are introduced by way of example that involve simple circuit design. The course will first introduce digital and computer systems and information representation. The course will then introduce the following topics: logic gates, boolean algebra, Karnaugh maps, design hierarchy, combinational circuit analysis and design, sequential circuit concepts and design, random access memory and programmable logic, algorithmic state machines (ASM) for controlling operations. Introductions to the hardware description languages, VHDL and Verilog, are provided with the expectation that at most one of the languages will be covered.

Main Topics To Be Covered:

- Digital Computers and Information.
- Combinational Logic Design.
- Sequential Logic Design.
- Memory and Programmable Logic Devices.
- Hardware Descriptive Languages (VHDL).
- Data Path.
- Finite State Machines (Sequencing and Control).

Relationships to other Courses & Labs:

ENGG*2410 and its lab will teach you plenty about digital hardware, its specification, design and implementation. More importantly however, is that it prepares you for lower level hardware description languages (HDL) and their use in digital design. Several other courses in the curriculum expand on ENGG*2410:

- **ENGG*3380, Embedded Architecture Design:** This course concentrates on the issues that arise in engineering of larger digital systems. Its students are exposed to requirements specification, higher level hardware description languages, hardware/software co-design.
- **ENGG*3640, Microcomputer Interfacing:** This course focuses on system and interfacing issues in the design of microprocessor-based digital systems. Among others, the course covers concepts in data acquisition and embedded systems.

Resources

Please pay attention to the ENGG*2410 Digital Systems Design webpage on Courselink. You will find the following useful information:

- **Course Annoucements:** will be made through the website, including due dates, even schedules, etc.
- **Lecture Information:** All the lecture notes will be posted on the web page.

- **Lab Information:** The handouts for all the lab sessions will be available there. Resources regarding tutorials and links to web pages can be found there as well.
- **Assignments:** Download the assignments according to the schedule given in this handout. The solutions will be posted as indicated.
- **Exams:** Some midterms and finals of previous years will be made available as samples of exams.
- **Forum:** A place to discuss course material for students is provided, together with a place to ask the instructor and TAs questions for the benefit of the class.

Tentative Schedule

Week	Date	Lecture Material	# Lectures	Source
#1	Sep 12-Sep 16	Introduction to Digital Design	3 Lecs	Chapter 1,2
#2	Sep 19-Sep 23	Combinational Logic Circuits	3 Lecs	Chapter 2
#3	Sep 26-Sep 30	Combinational Logic Design	3 Lecs	Chapter 2,3
#4	Oct 03-Oct 07	Combinational Logic Design Examples	3 Lecs	Chapter 3
#5	Oct 10-Oct 14	Arithmetic Circuits	2 Lecs	Chapter 5
#6	Oct 17-Oct 21	Sequential Circuits	3 Lecs	Chapter 6
#7	Oct 24-Oct 28	Sequential Circuit Design Examples	3 Lecs	Chapter 6
#8	Oct 31-Nov 04	Registers and Counters	3 Lecs	Chapter 7
#9	Nov 07-Nov 11	RTL Register Transfer and Data Path	3 Lecs	Chapter 7
#10	Nov 14-Nov 18	Control and ASMs	3 Lecs	Chapter 8
#11	Nov 21-Nov 25	Memory	3 Lecs	Chapter 9
#12	Nov 28-Dec 01	Programmable Logic Devices	3 Lecs	Chapter 3

Assignments

There will be 10 assignments throughout the term. **Solve all problems** and hand in your assignment to the teaching assistant in the tutorial and you will get 5 marks. It is in your interest to solve all assignments alone without any help since many questions of the midterm and final exam will be based on these assignments. Solutions will be posted on the web every other week.

Item	Handed In	Due Date	Topic
Assign #1	(Week #1)	Week #2	Number Systems
Assign #2	(Week #2)	Week #3	Boolean Algebra
Assign #3	(Week #3)	Week #4	K-Map simplification
Assign #4	(Week #4)	Week #5	Combinational logic Design
Assign #5	(Week #5)	Week #7	Arithmetic Circuits
Assign #6	(Week #7)	Week #8	Sequential Circuits
Assign #7	(Week #8)	Week #9	Registers and Counters
Assign #8	(Week #9)	Week #10	Data Path Circuits
Assign #9	(Week #10)	Week #11	Algorithmic State Machines
Assign #10	(Week #11)	Week #12	Memory & Programmable Logic

Labs

ENG241 labs are an integral part of the course. The objectives of the laboratories are:

- to help you understand and assimilate the lecture material.
- to give you practical experience with the process of design and implementation of digital circuits.
- to teach you design entry based on Hardware Description Languages.

- to give you hands-on-experience with CAD tools for digital hardware development.

There will be 8 labs throughout the term. The following are the due dates.

Item	Takes Place	Due Date	Topic
Lab #0	(Week #02)	-	Introduction to Lab Equipment
Lab #1	(Week #03)	(Week #04)	Combinational Logic & TTL
Lab #2	(Week #04)	(Week #05)	ISE Schematic Capture Tutorial
Lab #3	(Week #05)	(Week #06)	ISE VHDL Design Entry Tutorial
Lab #4	(Week #06)	(Week #07)	Combinational Logic Design
Lab #5	(Week #07)	(Week #08)	Design with VHDL
Lab #6	(Week #08)	(Week #09)	Sequential Logic Design
Lab #7	(Week #09)	(Week #10)	Data Path Design
Lab #8	(Week #10)	(Week #11)	Algorithmic State Machines

Exams

Midterms and a Final Exam will be conducted on the dates as shown in the table below. The following is the exam and quiz schedule:

Item	Week	Date	Location	Time	Topic
Midterm	8	TBA	TBA	TBA	Topics on Weeks #1-7
Final Exam	14	Dec 15th	TBA	8:30 AM	Topics on Weeks #1-12

Evaluation

- It is important to note that the quizes, midterm and final exam will be based on the assignment problems, so it is definitely in your interest to seriously attempt to do them all **alone**.
- You will save much time if you thoroughly study the relevant sections of the lab handouts before attempting the experiments in the lab. Come to the lab. with a clear understanding of what you are meant to accomplish, or with clear questions, so that the teaching assistant can help you.

Topic	Weight	Details	Comments
Assignments	5 %	10 Assignments	Solve all problems and hand in during Tutorial
Quizes	5 %	2 Quizes	During Class or Tutorial
Labs	15 %	8 Labs	Preparation, report, questions asked by TA
Midterm	25 %	5 Questions	Material covered week 1-7
Final Exam	50 %	8 Questions	Some questions will be based on lab work

1. Two quizes will be given throughout the term. **If you miss a quiz without a medical excuse there will be no makeup.**
2. **In order to pass the course, students must pass both the laboratory and final exam course portions. Students must obtain a grade of 50% or higher on the exam portion of the course in order for the laboratory write-up portion of the course to count towards the final grade**

Communication and Electronic Submission

The course will facilitate electronic communication werever possible. Primary communication on course material is through course website at Courselink. For personal or confidential matters, please do not hessitate to contact the instructor by email (asavich@uoguelph.ca) or in person.

Lab reports and assignments are expected to be submitted through Courselink. Please watch the website for due dates and submission instructions as appropriate.

Lateness

The penalty for late lab reports is 25% of report grade per day, with maximum of 2 days lateness. Beyond 2 days late, lab reports submissions will not be considered. Assignments must be handed in on time, and will not be considered if late. Students must attend and complete all laboratory demonstrations in person. If a laboratory is missed due to illness or other extenuating circumstance, arrangements must be made with the teaching assistants to complete a make-up lab.

Academic Misconduct

If you have trouble with material presented, please make sure you address this ahead of deadlines. We will be more than happy to accommodate your learning needs. On the other hand, plagiarism is not welcome. The general idea is that it is better not to submit a work than to submit a reproduction of your peers' work.

Please refer to the regulations outlined in the Undergraduate Calendar regarding academic misconduct (http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-amisconduct.shtml). The policy for this course is zero tolerance for any form of academic misconduct.

Safety

To ensure your safety and the safety of others, please abide by the lab safety regulations. The lab coordinator will explain them to you during the first lab session.

Disclaimer

The instructor reserves the right to change any or all of the above in the event of appropriate circumstance, subject to University of Guelph Academic Regulations.

Course Road-map

ENGG*2410 "Digital Systems Design" will teach you how to specify, design, and implement digital hardware. It will expose you to the basic concepts, representations, models, methods, techniques, standard components and plans. It will also provide you with the required foundations in discrete mathematics. Three principle classes of digital circuits will be discussed: combinational, synchronous sequential and asynchronous.