ENGG*4560 Embedded System Design
Winter 2017

UNIVERSITY of GUELPH

School of Engineering

(Revision 0: January 09, 2017)

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1 INSTRUCTIONAL SUPPORT

1.1 Instructor

Instructor: Radu Muresan, Ph.D., P.Eng.
Office: RICH 2509, ext. 56730
Email: rmuresan@uoguelph.ca
Office hours: Fridays: 1 pm to 3:30 pm; Or by appointment

1.2 Lab Technician

Lab Instructor: Kevin Dong
Office: RICH 2506, ext. xxxx
Email: kdong@uoguelph.ca

Teaching Assistants

GTA	Email	Office Hours
None	NA	NA

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2 LEARNING RESOURCES

2.1 Course Website

Course material, news, announcements, and grades will be regularly posted to the ENGG*4560 CourseLink site and on my personal course webpage. You are responsible for checking the sites regularly.

2.2 Required Resources

[1] F. Vahid, R. Lysecky, Verilog for Digital Design, Wiley, 2007.

[2] T. Padmanabhan, B. Sundari, Design through Verilog HDL, Wiley, 2004.

[3] Michael J. Flynn, Wayne Luk, *Computer System Design, System-on-Chip*, Wiley, 2011

[4] P. R. Schaumont, A Practical Introduction to Hardware/Software Codesign, Springer, 2010

2.3 Additional Resources

Lecture Information: All lecture notes are posted on the ENGG*4560 CourseLink system (Week #1 to Week #12) under LECTURES module.

Lab Information: The ENGG*4560 Embedded Systems Design Lab Manual is posted on the ENGG*4560 CourseLink system under the LABORATORY module.

Assignments: The assignments are posted on the ENGG*4560 CourseLink system under the ASSIGNMENTS module.

Exams: Some solutions of previous midterm exams will be posted on the ENGG*4560 CourseLink system under the EXAM SOLUTIONS section. Also, after the midterm exam a complete solution of the exam with the marking scheme applied will be posted for your reference.

Miscellaneous Information: Other information related to embedded systems design will be posted on the web page.

2.4 Communication & Email

Please use lectures and lab help sessions as your main opportunity to ask questions about the course. Major announcements will be posted to the course website. **It is your responsibility to check the course website regularly.** As per university regulations, all students are required to check their <mail.uoguelph.ca> e-mail account regularly: e-mail is the official route of communication between the University and its student.

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3 ASSESSMENT

3.1 Dates and Distribution

Labs + Project: 50% (Mark Distribution as follows: Lab 1 Demo = 2%; Lab 2 Demo = 2%; Lab 3 Demo = 2%; Lab 4 Demo = 2%; Lab 5 Demo = 4%; Project Stage 1 Demo + Report = 18% (Demo = 10%, Report = 8%); Project Phase 2 Demo + Report = 20% (Demo = 10%, Report = 10%).

See section 5.4 below for due dates

Midterm Assignment: 10%

Due date: This assignment requires an individual Verilog problem implementation with demo and test questions. The assignment demo and test is set for the first week after the reading week.

Final Exam: 40%

April 21st, 2015: 7:00 pm – 9:p0 pm, Room RICH 2531

3.2 Course Grading Policies

Missed Assessments: If you are unable to meet an in-course requirement due to medical, psychological, or compassionate reasons, please email the course instructor. See the undergraduate calendar for information on regulations and procedures for Academic Consideration: http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-ac.shtml

Accommodation of Religious Obligations: If you are unable to meet an in-course requirement due to religious obligations, please email the course instructor at the start of the semester to make alternate arrangements. See the undergraduate calendar for information on regulations and procedures for Academic Accommodation of Religious Obligations: http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-accomrelig.shtml

Passing grade: In order to pass the course, you must meet the following conditions:

1. Students must finalize and submit all the labs and project (Demo + Report) and obtain a passing grade of 50% or higher in all the labs and projects. Also the students are required to have a good participation on the work evaluation form (+/- 10% variation max allowed). If the participation work is not good the student needs to do the lab again individually. A penalty of 10% will be applied on the new lab submission. The work evaluation form can be downloaded from the ENGG*4560 CourseLink system found under the LABORATORY module. If an overall grade of lower than 50% is obtained in any lab, the students need to arrange with the instructor a new demo and report submission. In this case, grade penalties of up to 10% will be applied as appropriate.
2. Obtain a passing overall grade of 40% or higher in the final exam or an overall average of 50% or higher for the midterm assignment and final exam combined.
3. If the course passing conditions 1 and 2 are not met then the final course grade will be 47% (the laboratory grades will not be considered).

Contesting marks: All laboratory and midterm exam marks must be contested within 2 day from the grade submission. Also the exam must be written in pen or ink for contest consideration.

Missed midterm exam: If you miss a test due to grounds for granting academic consideration or religious accommodation, you will need to arrange a makeup exam date with the instructor or other solution such as move the midterm exam weight to the final exam if that is appropriate.

Lab/Project Work: You must attend and complete all laboratories. If you miss a laboratory demo due to grounds for granting academic consideration or religious accommodation, arrangements must be made with the instructor to complete a makeup lab demo.

Late Lab/Project Reports: Late submissions of lab reports will be accepted only with the approval of the course instructor. However, penalties on late submissions of up to 20% will be applied. Applied penalties will be posted on ENGG*4560 CourseLink system.

4 AIMS, OBJECTIVES & GRADUATE ATTRIBUTES

4.1 Calendar Description

This course introduces the basic principles of embedded system design. It utilizes advanced hardware/software abstractions to help design complex systems. Topics include: design of embedded CPUs; embedded architecture cores; system-on-chip designs and integration using processor cores and dedicated core modules; embedded computing platforms; embedded programming design and analysis; processes and operating systems; networks for embedded systems; distributed embedded architectures; design examples that target robotics, automobile, and communication systems.

Prerequisite(s): ENGG*3380 or ENGG*3640
Corequisite(s): None

4.2 Course Aims

This course is a senior level course in electrical and computer engineering. The main goals of the course are: (1) to teach students the fundamental of Bluespec System Verilog (BSV) as a programming language used in the design of electronic systems such as system-on-chip, FPGAs, and embedded systems (2) to teach students the basics of system-on-chip architectures and the performance issues related to the design of system-on-chip (3) to teach students the basics of the embedded systems design through modeling and synthesis tools.

4.3 Learning Objectives

At the successful completion of this course, the student will have demonstrated the ability to:

1. Digital design using Verilog
2. Design simple system components using Verilog such as combinational logic, sequential logic
3. Design a complex system-on-chip application using Verilog such as datapath components, interfaces.
4. System-on-chip architecture principles
5. Design and modeling of components for system-on-chip design such as processors, memory, interconnect
6. Chip basic performance analysis such as time, area, power, reliability and configurability
7. Hardware/Software Interfaces
8. Embedded system design synthesis principles at system, software and hardware levels
9. Demonstrate and communicate embedded system design results
10. Present new research results in the field of embedded systems design
11. Use of embedded systems design tools

4.4 Graduate Attributes

Successfully completing this course will contribute to the following CEAB Graduate Attributes:

Graduate Attribute	Learning Objectives	Assessment
1. Knowledge Base for Engineering	1, 2, 3, 4, 5,	Exams, Labs/Projects

	6, 7, 8	
2. Problem Analysis	2, 3, 4, 6	Exams, Labs/Projects
3. Investigation	2, 3	Labs/Projects
4. Design	2, 3, 4, 6	Exams, Labs/Projects
5. Use of Engineering Tools	1, 3, 7, 8, 9, 11	Assignments, Labs/Projects
6. Communication	3, 9, 10	Labs/Projects/Presentation
7. Individual and Teamwork	3, 9, 10	Labs/Projects/Presentation
8. Professionalism	9, 10	Labs/Projects/Presentation
9. Impact of Engineering on Society and the Environment	-	-
10. Ethics and Equity	-	-
11. Environment, Society, Business, & Project Management	-	-
12. Life-Long Learning	2, 3, 9, 11	Labs/Projects/Presentation

4.5 Instructor's Role and Responsibility to Students

The instructor's role is to develop and deliver course material in ways that facilitate learning for a variety of students. All lecture notes plus various exercises, examples and referenced resources will be made available to students on CourseLink system in the appropriate module. However, these are not intended to be stand-alone course notes. During lectures, the instructor will expand and explain the content of notes and provide in class solutions to problems that supplement posted notes. Scheduled classes and labs will be the principal venue to provide information and feedback for tests and labs.

4.6 Students' Learning Responsibilities

Students are expected to take advantage of the learning opportunities provided during lectures and labs. In addition students are encouraged to consult the instructor and the TA during the scheduled office hours or to contact the instructor or TA for any help needed. Students, especially those having difficulty with the course content, should also make use of other resources recommended by the instructor. Students who do (or may) fall behind due to illness, work, or extra-curricular activities are advised to keep the instructor informed. This will allow the instructor to recommend extra resources in a timely manner and/or provide consideration if appropriate.

4.7 Relationships with other Courses & Labs

Previous Courses:

ENGG*3640 (Microcomputer Interfacing): instruction set architecture, microcontroller architecture and design, interfacing principles and components.

Or ENGG*3380 (Computer Organization and Design): CPU design, instruction set design, microprocessor architectures and design, interfacing principles and components.

Follow-on Courses:

NA

5 TEACHING AND LEARNING ACTIVITIES

5.1 Timetable

Lectures:

Tuesday	Sec 01	1:00 pm – 2:20pm	MACK 238
Thursday	Sec 01	1:00 pm – 2:20pm	MACK 238

Laboratory:

Friday	Sec 01	12:30am – 3:20pm	RICH 2531

5.2 Lecture Schedule

Week	Lecture Topics	References	Learning Objectives
1	Combinational logic design with Verilog	[1]: Chapters 1-2	1, 2, 3
2	Sequential logic design with Verilog	[1]: Chapters 3	1, 2, 3
3	Datapath with Verilog	[1]: Chapters 4	1, 2, 3
4	RTL design with Verilog	[1]: Chapters 5	
5	System-on-chip design	[3]: Chapter 1	4
6	Chip basics performance analysis	[3]: Chapter 2	4, 6
7	Processors	[3]: Chapter 3	4, 5
8	Memory, Interconnect	[3]: Chapters 4, 5	4, 5
9	On-chip busses	[4]: Chapters 8	7, 8
10	Hardware/Software interfaces	[4]: Chapter 9	7, 8
11	Coprocessor control shell design	[4]: Chapters 10	7, 8, 11
12	Applications	[4]: Chapter 11	3, 11

5.3 Design Lab Schedule

Week	Activity	References	Learning Objectives
1	Lab safety presentation. Introduction to the embedded design tools.	Lab Manual	11
2	Lab1/Tutorial1: Libero Actel SOC Hardware Design. Decoder - Demo	Lab Manual	3, 4, 5, 8, 9, 11
3	Lab2/Tutorial2: Libero Actel SOC Hardware Design. PLL Clock - Demo	Lab Manual	3, 4, 5, 8, 9, 11
4	Lab3/Tutorial3: Libero Actel SOC Design. Creating Counter and PLL Designs Using Actel IP Cores - Demo	Lab Manual	3, 4, 5, 8, 9, 11
5	Lab4/Tutorial4: Libero Actel SOC Hardware Design. Verilog Counter - Demo	Lab Manual	3, 4, 5, 8, 9, 11
6	Lab5/Tutorial5: Libero Actel SOC Hardware Design. Memory Mapped I/O - Demo	Lab Manual	3, 4, 5, 8, 9, 11
7	Project Stage 1: Verilog Coprocessor Design – Implementation of the AES Encryption/Decryption Engine	Lab Manual	1, 2, 3, 5, 11
8	Project Stage 1 implementation	Lab Manual	3, 4, 9, 11
9	Project Stage 1 demo	Lab Manual	3, 4, 9, 11
10	Project Stage 2: SOC Design Projects – Implementation of the AES Encryption/Decryption Engine	Lab Manual	3, 4, 9, 11
11	Project Stage 2 demo	Lab Manual	3, 4, 9, 11

5.4 Lab Schedule

Week	Topic	Due
1	Introduction to Lab Equipment and Safety Training	
2	Lab1/Tutorial1: Libero Actel SOC Hardware Design. Decoder – Demo	Week 2: Demo
3	Lab2/Tutorial2: Libero Actel SOC Hardware Design. PLL Clock - Demo	Week 3: Demo
4	Lab3/Tutorial3: Libero Actel SOC Design. Creating Counter and PLL Designs Using Actel IP Cores – Demo	Week 4: Demo
5	Lab4/Tutorial4: Libero Actel SOC Hardware Design. Verilog Counter – Demo	Week 5: Demo
6	Lab5/Tutorial5: Libero Actel SOC Hardware Design. Memory Mapped I/O – Demo	Week 6: Demo
7- 9	Project Stage 1: Verilog Coprocessor Design Project	Week 9: Demo Week 9: Report
9-11	Project Stage 2: SOC Design Project	Week 11: Demo

Week 12: Report

5.5 Other Important Dates

Monday, 9 January 2017: First class
March xx, 2017: drop date – 40th class
April xx, 2017: last day of class
You can refer the student undergraduate calendars for the semester scheduled dates.

6 LAB SAFETY

Safety is critically important to the School and is the responsibility of all members of the School: faculty, staff and students. As a student in a lab course you are responsible for taking all reasonable safety precautions and following the lab safety rules specific to the lab you are working in. In addition, you are responsible for reporting all safety issues to the laboratory supervisor, GTA or faculty responsible.

7 ACADEMIC MISCONDUCT

The University of Guelph is committed to upholding the highest standards of academic integrity and it is the responsibility of all members of the University community faculty, staff, and students to be aware of what constitutes academic misconduct and to do as much as possible to prevent academic offences from occurring. University of Guelph students have the responsibility of abiding by the University's policy on academic misconduct regardless of their location of study; faculty, staff and students have the responsibility of supporting an environment that discourages misconduct. Students need to remain aware that instructors have access to and the right to use electronic and other means of detection.

Please note: Whether or not a student intended to commit academic misconduct is not relevant for a finding of guilt. Hurried or careless submission of assignments does not excuse students from responsibility for verifying the academic integrity of their work before submitting it. Students who are in any doubt as to whether an action on their part could be construed as an academic offence should consult with a faculty member.

7.1 Resources

The Academic Misconduct Policy is detailed in the Undergraduate Calendar:
http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-amisconduct.shtml

A tutorial on Academic Misconduct produced by the Learning Commons can be found at:
http://www.academicintegrity.uoguelph.ca/

Please also review the section on Academic Misconduct in your Engineering Program Guide.

The School of Engineering has adopted a Code of Ethics that can be found at:
http://www.uoguelph.ca/engineering/undergrad-counselling-ethics

8 ACCESSIBILITY

The University of Guelph is committed to creating a barrier-free environment. Providing services for students is a shared responsibility among students, faculty and administrators. This relationship is based on respect of individual rights, the dignity of the individual and the University community's shared commitment to an open and supportive learning environment. Students requiring service or accommodation, whether due to an identified, ongoing disability for a short-term disability should contact the Centre for Students with Disabilities as soon as possible.
For more information, contact CSD at 519-824-4120 ext. 56208 or email csd@uoguelph.ca or see the website: http://www.csd.uoguelph.ca/csd/

9 RECORDING OF MATERIALS

Presentations which are made in relation to course work—including lectures—cannot be recorded or copied without the permission of the presenter, whether the instructor, classmate or guest lecturer. Material recorded with permission is restricted to use for that course unless further permission is granted.

10 RESOURCES

The Academic Calendars are the source of information about the University of Guelph's procedures, policies and regulations which apply to undergraduate, graduate and diploma programs: http://www.uoguelph.ca/registrar/calendars/index.cfm?index