ENGG*4540 Advanced Computer Architecture
Winter 2014

UNIVERSITY of GUELPH

School of Engineering

(Revision 0: Jan 2, 201)

---

1 INSTRUCTIONAL SUPPORT

1.1 Instructor

Instructor: Fadi Al-Turjman, Ph.D.
Office: Richards 3513, ext. 54367
Email: fadi@uoguelph.ca
Office hours: By appointment @ Richards 3513

1.2 Lab Technician

Technician: Nathaniel Groendyk
Office: THRN 2308, ext. 53873
Email: groendyk@uoguelph.ca

1.3 Teaching Assistants

GTA	Email	Office Hours
Not applicable	-	-

---

2 LEARNING RESOURCES

2.1 Course Website

Course material, news, announcements, and grades will be regularly posted to the ENGG*4540 Courselink site. You are responsible for checking the site regularly.

2.2 Required Resources

[1] In class lecture notes and slides.

[2] John L. Hennessy and David A. Patterson**, "Computer Architecture: A Quantitative Approach"**, *5th Edition, Morgan Kaufmann Publishers*, ISBN 978-0-12-383872-8.

2.3 Recommended Resources

[3] http://www.digilentinc.com/Products/Detail.cfm?Prod=NEXYS3 .

[4] VHDL Handbook

2.4 Additional Resources

Lecture Information: All the lecture notes will be posted on the web page as we progress (week #1-#12).

Lab Information: The handouts for all the lab sessions are within the lab section. All types of resources regarding tutorials, links to web pages can be found in this section.

Assignments: All assignments will be announced/posted on the courselink (if any). Any new assignment will be announced on the due date of the previous one. Download the assignments and submit them according to the schedule given in this handout.

Exams: Selected questions/answers from midterms and finals of previous years will be reviewed during the course lectures as we progress.

Miscellaneous Information: Other information is posted on the web page.

2.5 Communication & Email Policy:

Please use lectures and lab help sessions as your main opportunity to ask questions about the course. Major announcements will be posted to the course website. **It is your responsibility to check the course website regularly.** As per university regulations, all students are required to check their <uoguelph.ca> e-mail account regularly: e-mail is the official route of communication between the University and its student.

---

3 ASSESSMENT

3.1 Dates and Distribution

Labs: 30%

Safety quiz: *on Friday Jan 10, 2014*

Lab reports: 8%

Report # 1: due on Friday Jan 31, 2014 (4%)

Report # 2: due on Friday Feb 14, 2014 (4%)

Report # 3: due on Friday Feb 28, 2014 (4%)

Project: 22%

Project proposal & presentation: due on Tuesday Feb 4, 2014 (2%)

Demo: on Friday April 4, 2014 (5%)

Final report: due on Monday April 7, 2014 (15%)

Note: both paper and electronic copies are to be submitted.

Quizzes: 15%

Quiz # 1: on Thursday January 30, 2014 (5%)

Quiz # 2: on Thursday February 27, 2014 (5%)

Quiz # 3: on Thursday March 27, 2014 (5%)

Midterm Exam: 20%

Thursday March 4, 2014 @ 8:30-10:00 am, Room MACK 305.

Final Exam: 35%

Wednesday April 16, 2014 @ 7:00-9:00 pm, Room TBA on Webadvisor.

3.2 Course Grading Policies

Missed Assessments: If you are unable to meet an in-course requirement due to medical, psychological, or compassionate reasons, please email the course instructor. See the undergraduate calendar for information on regulations and procedures for Academic Consideration: http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-ac.shtml

Accommodation of Religious Obligations: If you are unable to meet an in-course requirement due to religious obligations, please email the course instructor at the start of the semester to make alternate arrangements. See the undergraduate calendar for information on regulations and procedures for Academic Accommodation of Religious Obligations: http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-accomrelig.shtml

Passing grade: In order to pass the course, you must pass both the laboratory and exam course portions. Students must obtain a grade of 50% or higher on the exam portion of the course in order for the laboratory write-up portion of the course to count towards the final grade.

Missed midterm tests: If you miss a test due to grounds for granting academic consideration or religious accommodation, the weight of the missed test will be added to the final exam. There will be no makeup midterm tests.

Lab Work: You must attend and complete all laboratories. If you miss a laboratory due to grounds for granting academic consideration or religious accommodation, arrangements must be made with the instructor to complete a makeup lab.

Late Lab Reports: Late submissions of lab reports will not be accepted.

---

4 AIMS, OBJECTIVES & GRADUATE ATTRIBUTES

4.1 Calendar Description

This course covers topics such as: basics of pipeline structure, advanced pipelining and instruction level parallelism, multiprocessor and thread-level parallelism, memory-hierarchy design (main memory, virtual memory, caches), storage systems, interconnection networks, multiprocessor architectures (centralized and distributed). Advanced topics related to new emerging computer architectures will also be presented. The emphasis in each topic is on fundamental limitations and the trade-offs involved in designing computer systems, including memory and processing bandwidth, network bandwidth and latency, synchronization, and storage system bandwidth and latency.

Prerequisite(s): ENGG*3210, ENGG*3380.

4.2 Course Aims

The objective is to gain familiarity with computer architectures and their up-to-date applications, which are fundamental elements in computer engineering. The course will start with the quantitative principles of computer design. Then the course will present the instruction set principles and examples, in addition to overviewing advanced pipelining. Then, it will cover the instruction/data -level parallelism. Other topics to be covered, as well, are caching and storage systems design.

4.3 Learning Objectives

At the successful completion of this course, the student will have demonstrated the ability to:

1. Identify the task of a computer designer, technology and computer usage trends, cost and trends in cost, in addition to measuring and reporting performance of computer architectures.
2. Classify the instruction set architectures, and comprehend the instruction formats and semantics.
3. Identify and analyze basic pipeline operations, data and control pipeline hazards, and instruction-level parallelism.
4. Communicate effectively about advanced computer architectures and memory-hierarchy design; including cache design issues and performance evaluation techniques.
5. Comprehend and describe storage systems including types of storage devices, buses-connecting I/O devices to CPU/Memory, and the interfacing to an Operating System (OS).

4.4 Graduate Attributes

Successfully completing this course will contribute to the following CEAB Graduate Attributes:

Graduate Attribute	Learning Objectives	Assessment
1. Knowledge Base for Engineering	1	Tests and lab experiments.
2. Problem Analysis	1, 2	Lab project and experiments.
3. Investigation	3, 4, 5	Lab project and experiments.
4. Design	1, 3, 4, 5	Lab project and experiments, and tests.
5. Use of Engineering Tools	1, 4	Lab experiments.
6. Communication	4	Project report, project demonstration, and presentations.
7. Individual and Teamwork	1, 4	Tests, presentations, and lab project and experiments.
8. Professionalism	1, 4, 5	Lab project and experiments, project demonstration, and presentations.
9. Environment, Society, Business, & Project Management	1, 3, 4	Lab project and tests.
10. Life-Long Learning	1	Tests, presentations, lab project and experiments.

4.5 Instructor's Role and Responsibility to Students

The instructor's role is to develop and deliver course material in ways that facilitate learning for a variety of students. Selected lecture notes will be made available to students on Courselink/D2L but these are not intended to be stand-alone course notes. During lectures, the instructor will expand and explain the content of notes and provide example problems that supplement posted notes. Scheduled classes will be the principal venue to provide information and feedback for tests and project.

4.6 Students' Learning Responsibilities

Students are expected to take advantage of the learning opportunities provided during lectures and lab tutorials. Students, especially those having difficulty with the course content, should also make use of other resources recommended by the instructor. Students who do (or may) fall behind due to illness, work, or extra-curricular activities are advised to keep the instructor informed. This will allow the instructor to recommend extra resources in a timely manner and/or provide consideration if appropriate.

4.7 Relationships with other Courses & Labs

Previous Courses:

ENGG*3210: Computer network architectures, in-network caching and data dissemination.

ENGG*3380: Internal bus structure, registers, control sequence design, microprogramming and memory organization.

Follow-on Courses:

- Not Applicable.

5 TEACHING AND LEARNING ACTIVITIES

5.1 Timetable

Lectures:

Tue	8:30 – 9:50	MACK 305
Thu	8:30 – 9:50	MACK 305

Tutorials:

-

Laboratory:

Fri	12:30 - 2:30	RICH 1532

5.2 Lecture Schedule

Lecture	Lecture Topics	References	Learning Objectives
1-2	Introduction	[1][2]	1
3-6	Fundamentals of Quantitative Design and Analysis	[1][2]	1, 2
7-10	Memory Hierarchy Design	[1][2]	4, 5
11-14	Instruction-Level Parallelism and Its Exploitation	[1][2]	2, 3
15-18	Data-Level Parallelism in Vector, SIMD, and GPU Architectures	[1][2]	1, 2, 3
19-22	Multiprocessors	[1][2]	3, 4, 5
21-24	Warehouse-Scale Computers and Presentations	[1][2]	1, 3, 5

5.3 Design Lab Schedule

Week	Activity	References
1-2	Introduce the Nexys FPGA's development board.	[3][4]
3-4	Introduce Xilinx Embedded Development Kit (EDK) and VHDL.	[3][4]
5-6	Use Digilent Nexys board with LCD, PMODDA2, PMODAD1 and/or other peripherals.	[3][4]
7-11	Develop and implement an FPGA-based compueting architecture.	[3][4]

12	Lab project discussion and demonstration.	-

5.4 Lab Schedule

Week	Topic	Due
1-2	Introduce the Nexys development board.	Jan 31, 2014
3-4	Introduce Xilinx Embedded Development Kit (EDK) and VHDL.	Feb 14, 2014
5-6	Use Digilent Nexys board with LCD, PMODDA2, PMODAD1 and/or other peripherals.	Feb 28, 2014
7-9	Develop and implement an FPGA-based compueting architecture.	-
10-11	Lab project discussions.	-
12	Final project demo.	April 4, 2014

5.5 Other Important Dates

- Monday Jan 6, 2014: First class
- Monday, Feb 16, 2014: Winter break starts (1 week)
- Friday April 4, 2014: classes conclude.
- Students are also encouraged to check the undergraduate calendars for other semester scheduled dates.

6 LAB SAFETY

Safety is critically important to the School and is the responsibility of all members of the School: faculty, staff and students. As a student in a lab course you are responsible for taking all reasonable safety precautions and following the lab safety rules specific to the lab you are working in. In addition, you are responsible for reporting all safety issues to the laboratory supervisor, GTA or faculty responsible. Please refer to your lab manual for further safety instructions.

7 ACADEMIC MISCONDUCT

The University of Guelph is committed to upholding the highest standards of academic integrity and it is the responsibility of all members of the University community faculty, staff, and students to be aware of what constitutes academic misconduct and to do as much as possible to prevent academic offences from occurring. University of Guelph students have the responsibility of abiding by the University's policy on academic misconduct regardless of their location of study; faculty, staff and students have the

responsibility of supporting an environment that discourages misconduct. Students need to remain aware that instructors have access to and the right to use electronic and other means of detection.

Please note: Whether or not a student intended to commit academic misconduct is not relevant for a finding of guilt. Hurried or careless submission of assignments does not excuse students from responsibility for verifying the academic integrity of their work before submitting it. Students who are in any doubt as to whether an action on their part could be construed as an academic offence should consult with a faculty member.

7.1 Resources

The Academic Misconduct Policy is detailed in the Undergraduate Calendar:
http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-amisconduct.shtml

A tutorial on Academic Misconduct produced by the Learning Commons can be found at:
http://www.academicintegrity.uoguelph.ca/

Please also review the section on Academic Misconduct in your Engineering Program Guide.

The School of Engineering has adopted a Code of Ethics that can be found at:
http://www.uoguelph.ca/engineering/undergrad-counselling-ethics

8 ACCESSIBILITY

The University of Guelph is committed to creating a barrier-free environment. Providing services for students is a shared responsibility among students, faculty and administrators. This relationship is based on respect of individual rights, the dignity of the individual and the University community's shared commitment to an open and supportive learning environment. Students requiring service or accommodation, whether due to an identified, ongoing disability for a short-term disability should contact the Centre for Students with Disabilities as soon as possible.

For more information, contact CSD at 519-824-4120 ext. 56208 or email csd@uoguelph.ca or see the website: http://www.csd.uoguelph.ca/csd/

9 RECORDING OF MATERIALS

Presentations which are made in relation to course work—including lectures—cannot be recorded or copied without the permission of the presenter, whether the instructor, classmate or guest lecturer. Material recorded with permission is restricted to use for that course unless further permission is granted.

10 RESOURCES

The Academic Calendars are the source of information about the University of Guelph's procedures, policies and regulations which apply to undergraduate, graduate and diploma programs: http://www.uoguelph.ca/registrar/calendars/index.cfm?index