ENGG*4550 VLSI Digital Design
Winter 2014

UNIVERSITY of GUELPH

School of Engineering

(Revision 0: January 5, 2015)

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1 INSTRUCTIONAL SUPPORT

1.1 Instructor

Instructor: Radu Muresan, Ph.D., P.Eng.
Office: RICH 2509, ext. 56730
Email: rmuresan@uoguelph.ca
Office hours: Fridays: 1 pm to 3:30 pm; Or by appointment

1.2 Lab Technician

Technician: Joel Best
Office: RICH 3501, ext. 54234
Email: jbest@uoguelph.ca

1.3 Teaching Assistants

GTA	Email	Office Hours
None	NA	NA

2 LEARNING RESOURCES

2.1 Course Website

Course material, news, announcements, and grades will be regularly posted to the ENGG*4550 CourseLink site and on my personal course webpage. You are responsible for checking the sites regularly.

2.2 Required Resources

1. Neil H. E. Weste, David M. Harris, *CMOS VLSI Design A Circuits and System Perspective*, 4th Edition, Addison Wesley.
2. Radu Muresan, *Engg*4550 VLSI Digital Design Lab Manual*, University of Guelph, 2013.

2.3 Recommended Resources

1. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, Digital Integrated Circuits A Design Perspective, 2nd Edition, Pearson, 2003.

2.4 Additional Resources

Lecture Information: All lecture notes are posted on the ENGG*4550 CourseLink system (Week #1 to Week #12) under ENGG4550 LECTURES module.

Lab Information: The Engg*4550 VLSI Digital Design Lab Manual is posted on the ENGG*4550 Courselink system under the LABORATORY module.

Assignments: The assignments are posted on the ENGG*4550 CourseLink system under the ASSINGMENTS module.

Exams: Some solutions of previous midterm exams will be posted on the ENGG*4550 CourseLink system under the EXAM SOLUTIONS section. Also, after the midterm exam a complete solution of the exam with the marking scheme applied will be posted for your reference.

Miscellaneous Information: Other information related to VLSI digital design systems will be posted on the web page.

2.5 Communication & Email

Please use lectures and lab help sessions as your main opportunity to ask questions about the course. Major announcements will be posted to the course website. **It is your responsibility to check the course website regularly.** As per university regulations, all students are required to check their <mail.uoguelph.ca> e-mail account regularly: e-mail is the official route of communication between the University and its student.

3 ASSESSMENT

3.1 Dates and Distribution

Labs: 50%

- Lab 1 and Lab 2 are worth 10% each (Demo is 4% and report is 6%)
- Lab 3 and Lab 4 are worth 15% each (Demo is 6% and report is 9%)

Midterm Exam: 20%
Thursday, week after reading week: 7 pm – 9 pm, Room RICH 2531

Final Exam: 30%
April 10th, 2015: 2:30 pm to 4:30 pm, Room RICH 2531

3.2 Course Grading Policies

Missed Assessments: If you are unable to meet an in-course requirement due to medical, psychological, or compassionate reasons, please email the course instructor. See the undergraduate calendar for information on regulations and procedures for Academic Consideration: http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-ac.shtml

Accommodation of Religious Obligations: If you are unable to meet an in-course requirement due to religious obligations, please email the course instructor at the start of the semester to make alternate arrangements. See the undergraduate calendar for information on regulations and procedures for Academic Accommodation of Religious Obligations: http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-accomrelig.shtml

Passing grade: In order to pass the course, you must meet the following conditions:

1. Students must finalize and submit all the labs and projects (Demo + Report) and obtain a passing grade of 50% or higher in all the labs and projects. Also the students are required to have a good participation on the work evaluation form (+/- 10% variation max allowed). In case the participation is not good then the student must redo the lab (demo and report) individually and submit it for marking. The work evaluation form can be downloaded from the Engg*4550 CourseLink system found under the LABORATORY module. If an overall grade of lower than 50% is obtained in any lab, the students need to arrange with the instructor a new demo and report submission. In this case, a grade penalty of 10% deduction will be applied.
2. Obtain a passing grade of 50% or higher in the final exam or an average of 50% or higher for the midterm exam and final exam [that is: (midterm exam + final exam)/2 ≥ 50%].
3. If the course passing conditions 1 and 2 are not met then the final course grade will be the average of the exams out of 100% (the laboratory grades will not be considered).

Contesting marks: All laboratory and midterm exam marks must be contested within 2 days from the grade submission. Also the exam must be written in pen or ink for contest consideration.

Missed midterm exam: If you miss a test due to grounds for granting academic consideration or religious accommodation, you will need to arrange a makeup exam date with the instructor.

Lab Work: You must attend and complete all laboratories. If you miss a laboratory demo due to grounds for granting academic consideration or religious accommodation, arrangements must be made with the instructor to complete a makeup lab demo.

Late Lab Reports: Late submissions of lab reports will be accepted only with the approval of the course instructor. However, penalties on late submissions of up to 20% will be applied. Applied penalties will be posted on Engg*4550 CourseLink system.

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4 AIMS, OBJECTIVES & GRADUATE ATTRIBUTES

4.1 Calendar Description

This course introduces the students to the analysis, synthesis and design of Very Large Scale integration (VLSI) digital circuits and implementing them in silicon. The topics of this course are presented at three levels of design abstraction. At device level: MOS diode, MOS (FET) transistor, interconnect wire. At circuit level: CMOS inverter, static CMOS gates (NAND, NOR), dynamic gates (NAND, NOR), static latches and registers, dynamic latches and registers, pipelining principles and circuit styles, BICMOS logic circuits. At system level: implementation strategies for digital ICs, interconnect at system level, timing issues in digital circuits (clock structures), the adder, the multiplier, the shifter, memory design and array structure, low power design circuits and architectures. Also, issues related to delay, power and robustness will be presented at these three design abstraction levels.

Prerequisite(s): ENGG*2410, ENGG*2450, ENGG*3450
Corequisite(s): None

4.2 Course Aims

This course is a senior level course in electrical and computer engineering. The main goals of the course are: (1) to teach students the fundamentals of the VLSI digital design at all levels of design abstraction (i.e., physical design, circuit design, logic design, microarchitecture design, and architecture design), (2) to teach students the importance of the key factors in the VLSI design (i.e., delay, power, interconnect, and robustness).

4.3 Learning Objectives

At the successful completion of this course, the student will have demonstrated the ability to:

1. Understand the MOS transistor theory and MOS transistor models for VLSI design.
2. Understand the CMOS process technology and the CMOS chip fabrication rules and steps.
3. Use chip design metrics such as delay, speed, power and robustness for VLSI designs.
4. Analyze and evaluate power at various levels of design abstraction in VLSI integrated chips.
5. Model the interconnect and basic components.
6. Design combinational and sequential circuits.
7. Design datapath subsystems such as adders, comparators, and multipliers.
8. Understand the basics of memory design for SRAM, DRAM and ROM.
9. Use simulation and fabrication tools for nanoscale VLSI designs.
10. Design gates and datapath subsystem using the TSMC 65 nm technology process.

11. Demonstrate and communicate VLSI system design results.

4.4 Graduate Attributes

Successfully completing this course will contribute to the following CEAB Graduate Attributes:

Graduate Attribute	Learning Objectives	Assessment
1. Knowledge Base for Engineering	1, 2, 3, 4, 5, 6, 7, 8	Exams, Labs
2. Problem Analysis	3, 4, 6, 7, 9	Exams, Labs
3. Investigation	9, 10	Labs
4. Design	2, 3, 4, 6, 7, 8, 11, 9, 10	Exams, Labs
5. Use of Engineering Tools	9, 10, 11	Labs
6. Communication	9,10, 11	Labs
7. Individual and Teamwork	9, 10, 11	Labs
8. Professionalism	11	Labs
9. Impact of Engineering on Society and the Environment	2	Exams
10. Ethics and Equity	-	-
11. Environment, Society, Business, & Project Management	-	-
12. Life-Long Learning	2, 9, 10	Labs

4.5 Instructor's Role and Responsibility to Students

The instructor's role is to develop and deliver course material in ways that facilitate learning for a variety of students. All lecture notes plus various exercises, examples and referenced resources will be made available to students on CourseLink system in the appropriate module. However, these are not intended to be stand-alone course notes. During lectures, the instructor will expand and explain the content of notes and provide in class solutions to problems that supplement posted notes. Scheduled classes and labs will be the principal venue to provide information and feedback for tests and labs.

4.6 Students' Learning Responsibilities

Students are expected to take advantage of the learning opportunities provided during lectures and labs. In addition students are encouraged to consult the instructor and the TA during the scheduled office hours or to contact the instructor or TA for any help needed. Students, especially those having difficulty with the course content, should also make use of other resources recommended by the instructor. Students who do (or may) fall behind due to illness, work, or extra-curricular activities are advised to keep the instructor informed. This will allow the instructor to recommend extra resources in a timely manner and/or provide consideration if appropriate.

4.7 Relationships with other Courses & Labs

Previous Courses:

ENGG*2410 (Digital Systems Design Using Descriptive Language): Boolean algebra, design synthesis and realization of combinational and sequential circuits, hardware testing.

ENGG*2450 (Electric Circuits): Fundamentals of electric circuit analysis, circuit elements, DC current analysis, linearity and superposition principles, circuit theorems.

ENGG*3450 (Electrical Devices): Semiconductor materials, diodes, transistors, electronic components and circuit analysis.

Follow-on Courses:

NA

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5 TEACHING AND LEARNING ACTIVITIES

5.1 Timetable

Lectures:

Monday	Sec 01	4:00 pm – 5:20 pm	MACS 301
Friday	Sec 01	4:00 pm – 5:20 pm	MACS 301

Laboratory:

Friday	Sec 01	10:30 am - 12:20 pm	RICH 2531

5.2 Lecture Schedule

Week	Lecture Topics	References	Learning Objectives
1	MOS transistor theory and VLSI design abstraction levels	Chapters 1, 2	1
2	CMOS processing technology. RC delay models	Chapters 3, 4	2, 3
3	Linear delay model. Logical effort	Chapter 4	3
4	Power in VLSI integrated circuits	Chapter 5	3, 4
5	Interconnect. Robustness	Chapter 6, 7	5, 3
6	Combinational circuit design 1	Chapter 9	6, 3, 4
7	Combinational circuit design 2	Chapter 9	6, 3, 4
8	Sequential circuit design	Chapter 10	6, 3, 4
9	Datapath subsystems. Adders	Chapter 11	7, 3, 4
10	Datapath subsystems. Multipliers	Chapter 11	7, 3, 4
11	Array subsystems. Memory design	Chapter 12	8, 3, 4
12	Special purpose subsystems	Chapter 13	7

5.3 Design Lab Schedule

Week	Activity	References	Learning Objectives
1	Lab safety presentation. Introduction to Lab 1 design requirements and Cadence simulation tools.	Lab Manual	1, 3, 9
2-4	Lab 1 implementation, demo and report	Lab Manual	1, 3, 9, 11
4	Introduction to Lab 2 design requirements and Cadence simulation and analysis tools. Implementation	Lab Manual	6, 3, 9
5-6	Lab 2 implementation, demo and report.	Lab Manual	6, 3, 9, 11
6	Introduction to Lab 3 design requirements and layout tools	Lab Manual	2, 3, 6, 9, 10
8-10	Lab 3 implementation, demo and report.	Lab Manual	2, 3, 6, 9, 10, 11
10	Introduction to Lab 4 design requirements. Implementation	Lab Manual	2, 3, 6, 7, 9, 10
11-12	Lab 4 implementation, demo and report.		2, 3, 6, 7, 9, 10, 11

5.4 Lab Schedule

Week	Topic	Due
1	Introduction to Lab Equipment and Safety Training	
1-3	Lab 1: Using Virtuoso Cadence to simulate an RLC circuit, an NMOS transistor, and an inverter. Equivalent resistance and capacitance simulation, analysis and calculations.	Week 3: Demo Week 3: Report
4-5	Lab 2: Using Virtuoso Cadence to simulate and analyze an NAND2 gate. Creating symbols, building the testbench, using the calculator. Logical effort analysis circuit.	Week 5: Demo Week 5: Report
6-7	Lab 3: Layout of an inverter gate using the 65 nm TSMC process. LVS, DRC, post layout simulation and verification.	Week 7: Demo Week 7: Report
8-9	Lab 4: Build a custom cell library for designing a small datapath subsystem using the 65 nm TSMC process.	Week 9: Demo
8-12	Project: Design a datapath subsystem using the custom cell library developed in Lab 4. Design, layout, LVS, DRC, post layout simulation. Circuit analysis report.	Week 12: Demo Week 12: Report

5.5 Other Important Dates

Friday, 5 January 2015: First class
Friday, March 6th: drop date – 40th class
Friday, April 2nd, 2015: last day of class
You can refer the student undergraduate calendars for the semester scheduled dates.

6 LAB SAFETY

Safety is critically important to the School and is the responsibility of all members of the School: faculty, staff and students. As a student in a lab course you are responsible for taking all reasonable safety precautions and following the lab safety rules specific to the lab you are working in. In addition, you are responsible for reporting all safety issues to the laboratory supervisor, GTA or faculty responsible.

7 ACADEMIC MISCONDUCT

The University of Guelph is committed to upholding the highest standards of academic integrity and it is the responsibility of all members of the University community faculty, staff, and students to be aware of what constitutes academic misconduct and to do as much as possible to prevent academic offences from occurring. University of Guelph students have the responsibility of abiding by the University's policy on academic misconduct regardless of their location of study; faculty, staff and students have the responsibility of supporting an environment that discourages misconduct. Students need to remain aware that instructors have access to and the right to use electronic and other means of detection.

Please note: Whether or not a student intended to commit academic misconduct is not relevant for a finding of guilt. Hurried or careless submission of assignments does not excuse students from responsibility for verifying the academic integrity of their work before submitting it. Students who are in any doubt as to whether an action on their part could be construed as an academic offence should consult with a faculty member.

7.1 Resources

The Academic Misconduct Policy is detailed in the Undergraduate Calendar:
http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-amisconduct.shtml

A tutorial on Academic Misconduct produced by the Learning Commons can be found at:
http://www.academicintegrity.uoguelph.ca/

Please also review the section on Academic Misconduct in your Engineering Program Guide.

The School of Engineering has adopted a Code of Ethics that can be found at:
http://www.uoguelph.ca/engineering/undergrad-counselling-ethics

8 ACCESSIBILITY

The University of Guelph is committed to creating a barrier-free environment. Providing services for students is a shared responsibility among students, faculty and administrators. This relationship is based on respect of individual rights, the dignity of the individual and the University community's shared

commitment to an open and supportive learning environment. Students requiring service or accommodation, whether due to an identified, ongoing disability for a short-term disability should contact the Centre for Students with Disabilities as soon as possible.
For more information, contact CSD at 519-824-4120 ext. 56208 or email csd@uoguelph.ca or see the website: http://www.csd.uoguelph.ca/csd/

9 RECORDING OF MATERIALS

Presentations which are made in relation to course work—including lectures—cannot be recorded or copied without the permission of the presenter, whether the instructor, classmate or guest lecturer. Material recorded with permission is restricted to use for that course unless further permission is granted.

10 RESOURCES

The Academic Calendars are the source of information about the University of Guelph's procedures, policies and regulations which apply to undergraduate, graduate and diploma programs: http://www.uoguelph.ca/registrar/calendars/index.cfm?index