ENGG 3380 Computer Organization and Design
(formally Embedded Architecture Design)

Fall 2007

1 Teaching staff

⇒ **Instructor** Dr. Medhat Moussa

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2 Course Format and Organizational Details

The course will be delivered through 3 lectures/week. Labs will be used to help students learn VHDL and how it can be used in implementation of digital designs on FPGAs. Students will be required to complete a major design project that will include several design phases.

Lectures: MACK 031 MWF 11:30AM 12:20PM

Lab.: THRN 2307

Final Exam: Dec. 3, 2007

Course website: http://courselink.uoguelph.ca/

⇒ **Textbooks:**

1. D. A. Patterson and J.L. Hennessy, *Computer Organization and Design: The hardware/software interface*, 3nd ed. Morgan Kaufmann. (Main textbook)

Lectures will also include materials covered in the following texts for microprocessor design and implementation.

1. J.L. Hennessy and D. A. Patterson, *Computer Architecture: A Quantitative Approach*, 4th ed., Morgan Kaufmann

2. C. Hamacher, Z. Vranesic, S. Zaky, *Computer Organization*, 5*th* edition, McGraw Hill.

3. J. Carpinelli, *Computer Systems Organization and Architecture*, Addison Wesley.

4. W. Stallings, *Computer Organization and Architecture*. 5*th* edition, Prentice Hall

5. Morris Mano and C. Kime, *Logic And Computer Design Fundamentals,* 2nd Ed., Prentice Hall.

⇒ **Evaluation**

⇒ Project 45% (divided over several phases)

⇒ Lab report and assignments 10%

⇒ Final Exam 45%

3 Course Objective and Outline

3-1 Objectives

In this course, students will design, build and program a CPU for use in embedded applications. Topics include:

- ⇒ CPU Design: instruction set design; addressing modes; machine code; accessing operators and operands; stack, register, and memory approaches; instruction set program; hardwired control
- ⇒ Microprogramming: microprogrammed control; microarchitecture design
- ⇒ RISC vs. CISC designs: rationale; pipelining; ISP issues; optimization
- ⇒ Memory Management: cache memory; protection; partitioning, swapping; paging, segmentation; virtual memory (Time permits).
- ⇒ Other advanced subjects (Time permits).

3-2 Outline

Review of Technology Trends and Cost/Performance (Patterson, Ch2)	Week 1
Review of Technology Trends and Cost/Performance, Processor Performance Trends, The Task of a Computer Designer, Definition of Computer Architecture, Cost/Performance Analysis, Fundamental “Laws”/Principles, SPEC: System Performance Evaluation Cooperative, Amdal's Law	
Instruction Set Architecture (Patterson, Ch3)	Week 2-3
Introduction to MIPS ISA(Outside source), Alternative Architectures and ISA design factors, ISA and Machine Format Design	
CPU Design, Datapath (Hamacher, Ch9; Carpinelli, Ch6)	Week 4
Datapath Components, Register transfer Language, Complete instruction execution, Branch instruction, Multiple-Bus Organization	
CPU Design, Control (Hamacher, Ch9)	Week 5-6
Hardwired Control, Microprogramming Control	
Pipelining (Hennessy, Ch3)	Week 7-8
Pipeline Registers, Pipelining Hazards, Stalls, Structural hazards, Data hazards, Control Hazards, Control Implementation for Data Hazards, Delayed branches	
Advanced pipelining, Instruction Level Parallelism (ILP) (Hennessy, Ch4)	Week 9-10
Loop unrolling, Dependency, Data Dependency, Name Dependency, Control Dependency	
Advanced pipelining, Dynamic Scheduling (Hennessy, Ch4.2)	Week 11-12
Basic idea, Scoreboarding, Dynamic Hardware Prediction, Multiple issue Design	