ENGG3380
COMPUTER ORGANIZATION

INSTRUCTOR
RADU MURESAN

TEXT BOOK

- William Stallings, COMPUTER ORGANIZATION AND ARCHITECTURE, Designing for Performance; Pearson, Ninth Edition, 2012
- REASONS FOR CHOOSING THE TEXT BOOK
  1. The book relies on examples from two popular processor families: the Intel x86 and the ARM
  2. The book explains the fundamental functionality in each area presented.
  3. The book explores current techniques employed to achieve maximum performance.

COURSE SYLLABUS -- LECTURES

- CHAPTERS COVERED IN THE FOLLOWING ORDER:
  - Chapter 2: Computer Evolution and Performance
  - Chapter 12: Instruction Sets: Characteristics and Functions
  - Chapter 19: Control Unit Operation – Covered in the Labs as part of the CPU design
  - Chapter 13: Instruction Sets: Addressing Modes and Formats
  - Chapter 14: Processor Structure and Function
  - Chapter 15: Reduces Instruction Set Computers

COURSE SYLLABUS – LECTURES

- Chapter 16: Instruction Level Parallelism and Superscalar Processors
- Chapter 3: A Top-Level View of Computer Function and Interconnection
- Chapter 5: Internal Memory
- Chapter 4: Cache Memory
- Chapter 6: External Memory
- Chapter 7: Input/Output
- Chapter 8: Operating System Support

COURSE SYLLABUS – LECTURES

- Chapter 19: Control Unit Operation
- Chapter 20: Microprogrammed Control

- If the time allows the following two chapters will also be covered in class:
  - Chapter 17: Parallel Processing
  - Chapter 18: Multicore Computers

COURSE SYLLABUS – LAB - TBD

- LABS -- The Labs will cover the following:
  - Tutorial on the Xilinx development board
  - Tutorial on VHDL
  - Tutorial on CPU Implementation
  - Design Proposal – marked 10%
- PROJECT – The students will implement a final CPU project on the Xilinx board – marked 40%
  - Brakedown: 20% the report + 20% the demo

COURSE SYLLABUS – MARKING SCHEME

- MIDTERM – 25% -- Covers Part 1 of the course
- FINAL EXAM – 25% -- Covers Part 2 of the course
- NOTE: The Midterm and Final Exams are non-overlapping.
- Laboratory Work– 50%
  - Distribution :
    - Design Proposal (10%) -- 3 – 10 pages proposal.
    - Project Demo (20%) + Project Report (20%)
      - The Report should be: 15 – 25 pages the design plus xx pages for the VHDL code in the Appendix).
- COURSE PASSING CONDITION: Overall average of 50%