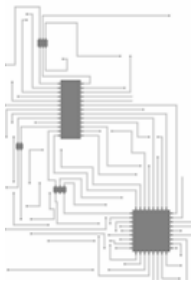
ENGG4550: VLSI Digital Design

Instructor: Radu Muresan

Weblink:

http://www.soe.uoguelph.ca/webfiles/rmuresan/ENG4550-VLSI.htm



References

- Text Book:
  - N. Weste, …, "CMOS VLSI Design, A Circuit and Systems Perspective," 3rd Edition, Addison, 2005.
- Other References:
  - J. M. Rabaey, …, "Digital Integrated Circuits, A Design Perspective" 2nd Edition, Prentice Hall, 2003.
  - S. Kang, …, "CMOS Digital Integrated Circuits, Analysis and Design," 3rd Edition, Mc Graw Hill, 2003.
  - Sedra/Smith, 5th Edition, Microelectronic Circuits, 2004

Course Outline (Tentative)

- Topic 1: MOS transistor, CMOS manufacturing process;
- Topic 2: CMOS Inverter; Static and Dynamic Behavior; Performance, Power and Energy Issues;
- Topic 3: Combinational Logic Gates;
- Topic 4: Designing Arithmetic Building Blocks
- Topic 5: Sequential Logic;
- Topic 6: Voltage scaling, frequency scaling, power and speed trades off;
- Topic 7: Verilog Integration;
- Topic 8: ASIC digital Design Flow;
- Topic 9: ASIC design case studies;
- Topic 10: Power Issues at System Level;

Tutorials

- Tutorial 1: Analyze a RLC Circuit, a nMOS Transistor, and an Inverter (0.18 um);
- Tutorial 2: Schematic Entry and Analog Simulation – NAND and Buffer Circuits;
- Tutorial 3: Layout Tutorial - Layout an Inverter in CMOSP18 Technology;
- Other Tutorials:
  - Tutorial 4 & 5: Adder Design Using Custom Cells and Standard Cell Library;
  - Tutorial 6: VHDL Simulation Using CMC Tools;
  - Tutorial 7: Synopsys Nanosim Simulation;

Presentations (Only for Graduate Students); Assignments

- Choose a journal paper related to your research area and to the VLSI course areas;
  - Suggested areas: power; custom design; ASIC design; standard cell design; CAD tools;
- Prepare a 15 minutes presentation on the topic – 12 to 16 slides;
- Assignments are grouped at the end of the Tutorials;

Project Ideas

- Complete Layout Design of a Type Selective 8-Bit Adder – custom cells design;
- Complete Layout Design of a Type Selective 8-Bit Adder – standard cells design;
- Develop Basic Custom Cells that Have Reduced Current to Data Dependency;
- DES or AES - custom cell or standard cell design;
- Propose your own project for approval;

Undergraduate Course Work, Marking Scheme

- Tutorial 1 + Assignment Set 1 due W4;
- Tutorial 2 + Assignment Set 2 due W6;
- Tutorial 3 + Assignment Set 3 due W8;
- Project due W12;
- Marking Scheme for ENGG4550:
  - Project – 20%;
  - Tutorials/Assignments – 30%
  - Midterm – 20%
  - Final Exam – 30%;
  - (?? Tentative) To apply the best of:
    - (Project 20, Final Exam 30) or (Project 30 Final Exam 20)

Graduate Course Work, Marking Scheme

- Tutorial 1 + Assignment Set 1 due W4;
- Tutorial 2 + Assignment Set 2 due W6;
- Tutorial 3 + Assignment Set 3 due W8;
- Marking Scheme for ENGG6520:
  - Project – 30%;
  - Tutorial/Assignments – 20%;
  - Presentation – 10%;
  - Final Exam (3 hours exam) – 40%;

Marks and Group Work

- All marks (except the final exam mark) must be contested within 3 working days from the submission date otherwise they will be finalized as submitted
- For all group work the students must complete one WORK EVALUATION FORM
  - The group marks will not be finalized without the evaluation form
  - The evaluation form can be downloaded from the course's webpage

QUESTIONS ???