ENGG*3050 Embedded Reconfigurable Computing Systems
Fall 2018

UNIVERSITY of GUELPH
School of Engineering

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1 Instructional Support

1.1 Course Instructor

Instructor:	Mohamad Abou El Nasr, Ph.D.
Office:	RICHS 1531, ext. 52447
Email:	mabouelN@uoguelph.ca
Office hours:	Mondays: 11:00 - 12:00 or By appointment

1.2 Lab Instructor/Coordinator

Instructor:	Matthew Saunders
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Email:	msaund05@uoguelph.ca

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2 Learning Resources

2.1 Course Website

Course material, news, announcements, and grades will be regularly posted to the ENGG*3050 Course Webpage site. You are responsible for checking the site regularly.

2.2 Required Resources

1. Edited by S. Hauck and A. Dehon *Reconfigurable Computing: The Theory and Practice of FPGA-Based Computing* Morgan Kaufmann, 2008, ISBN 978-0-12-370522.

2.3 Recommended Resources

1. "Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications", by C. Bobda Springer, 2008, ISBN 978-1-4020-6088-5.
2. "VHDL for Engineers", by K. Short, 2nd Edition, Prentice Hall, 2008.
3. "The Designer's Guide to VHDL", by Peter Ashenden, Morgan Kaufmann, 2002, ISBN 1-55860-674-2.

2.4 Additional Resources

1. Lecture Information: All the lecture notes are posted on the web page (week #1-#12).
2. Lab Information: The handouts for all the lab sessions are within the lab section. All types of resources regarding tutorials, links to web pages can be found in this section.
3. Assignments: Download the assignments according to the schedule given in this handout. All the solutions will be posted as indicated.
4. Exams: Some midterms and finals of previous years are posted as samples of exams. The solutions are also posted for your convenience.
5. Miscellaneous Information: Other information related to Reconfigurable Computing are also posted on the web page.

2.5 Communication & Email Policy

Please use lectures and lab help sessions as your main opportunity to ask questions about the course. Major announcements will be posted to the course website. **It is your responsibility to check the course website regularly**. As per university regulations, all students are required to check their "mail.uoguelph.ca" e-mail account regularly: e-mail is the official route of communication between the University and its student.

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3 ASSESSMENT

3.1 Dates and Distribution

1. Labs: 30%, See Section 5 for due dates
2. Project: 20%, See Section 5 for due dates
3. Paper Review: 10%
   Week 11, during the Lecture
4. Final Exam: 40%
   Thur. Dec. 13th, 2018 07:00PM - 09:00PM (Room TBA)

3.2 Course Grading Policies

Missed Assessments: If you are unable to meet an in-course requirement due to medical, psychological, or compassionate reasons, please email the course instructor. See the undergraduate calendar for information on regulations and procedures for Academic Consideration:
http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-ac.shtml

Accommodation of Religious Obligations: If you are unable to meet an in-course requirement due to religious obligations, please email the course instructor within two weeks of the start of the semester to make alternate arrangements. See the undergraduate calendar for information on regulations and procedures for Academic Consideration of Religious Obligations:
http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-accomrelig.shtml

Passing grade: In order to pass the course, you must pass both the project/laboratory and exam course portions. Students must obtain a grade of 50% or higher on the exam portion of the course in order for the project and laboratory write-up portion of the course to count towards the final grade.

Missed midterm/quiz tests: If you miss a test due to grounds for granting academic consideration or religious accommodation, the weight of any missed test will be added to the final exam weight. There will be **no makeup midterm tests**.

Lab Work: You must attend and complete all laboratories. If you miss a laboratory due to grounds for granting academic consideration or religious accommodation, arrangements must be made with the teaching assistant to complete a makeup lab.

Late Lab/Project Reports: Late submissions of lab reports will be penalized unless you have good reasons. Explain to the instructor and/or teaching assistant the circumstances of why your lab report is sumbitted late.

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4 AIMS, OBJECTIVES & GRADUATE ATTRIBUTES

4.1 Calendar Description

This course introduces the students to the analysis, synthesis and design of embedded systems and implementing them using Field Programmable Gate Arrays. Topics include: review of digital design concepts; Programmable Logic Devices; Field Programmable Logic Devices; physical design automation (partitioning, placement and routing); Hardware Descriptive Languages; VHDL; Verilog; High Level Languages; Vivado HLS; Fixed Point and Floating Point Arithmetic; Hardware Accelerators; Reconfigurable Instruction Set Computers; Hardware Software Co-design techniques; Application of Field Programmable Logic in Embedded Systems.
Prerequisite(s): ENGG*2410, ENGG*3380

4.2 Course Aims

Reconfigurable Computing Systems (RCS) refers to a new class of computer architecture which take advantage of application level-parallelism. This course deals mainly with digital systems implemented on Field Programmable Gate Arrays (FPGA). In this course, we investigate the state-of-the-art in reconfigurable computing and the main factors driving it. Initially, we review the basic concepts of programmable logic in general and FPGAs in particular. Design entry based on Hardware Descriptive Languages and High Level Languages will also be covered. Specific reconfigurable computing systems (i.e architectures) will be examined with emphasis on limitations and future research opportunities.

4.3 Learning Objectives

At the successful completion of this course, the student will have demonstrated the ability to:

1. Understand the basic concept of Reconfigurable Computing both from a hardware and software perspective.
2. Learn all details of digital hardware, its specification, analysis, design and implementation.
3. Get acquainted with both low level hardware description languages (HDL) and state of the art high level languages such as Vivado HLS.

4. Use different analysis and verification tools, implementation and synthesis methodologies and testability techniques that will enable them to design high performance and efficient digital systems.

5. Implement a complete digital system on FPGAs using state-of-the art CAD tools.

4.4 Graduate Attributes

Successfully completing this course will contribute to the following CEAB Graduate Attributes:

Graduate Attribute	Learning Objectives	Assessment
1. Knowledge Base for Engineering	1, 2, 4, 5	Exams, Project
2. Problem Analysis	2, 3, 4	Exams, Project
3. Investigation	3, 4, 5	Labs
4. Design	2, 3, 4, 5	Labs, Exams, Project
5. Use of Engineering Tools	3, 4, 5	Labs, Project
6. Communication	3, 4, 5	Labs
7. Individual and Teamwork	3, 4, 5	Labs
8. Professionalism	2, 3,	-
9. Impact on Society and Environment	1	Exams, Project
10. Ethics and Equity	3, 4, 5	Labs, Exams
11. Environment, Society, & Project Management	3, 4, 5	Labs
12. Life-Long Learning	5	-

4.5 Instructor's Role and Responsibility to Students

The instructor's role is to develop and deliver course material in ways that facilitate learning for a variety of students. Selected lecture notes will be made available to students on Course-link/D2L but these are not intended to be stand-alone course notes. During lectures, the instructor will expand and explain the content of notes and provide example problems that supplement posted notes. Scheduled classes will be the principal venue to provide information and feedback for tests and project.

4.6 Students' Learning Responsibilities

Students are expected to take advantage of the learning opportunities provided during lectures and tutorials. Students, especially those having difficulty with the course content, should also make use of other resources recommended by the instructor. Students who do (or may) fall behind due to illness, work, or extra-curricular activities are advised to keep the instructor informed. This will allow the instructor to recommend extra resources in a timely manner and/or provide consideration if appropriate.

4.7 Relationships with other Courses

ENGG*3050 and its lab will teach you plenty about digital hardware, its specification, design and implementation. More importantly however, is that it prepares you for lower level hardware description languages (HDL) and their use in computer architecture. The course prerequisites ENGG*2410 and ENGG*3640 are essential for the following reasons:

- **ENGG*2410, Digital Design:** This course is an introductory course in digital logic design, which is a basic course in most electrical and computer engineering programs. ENGG*2410 covers both combinational logic and sequential logic design. It also covers datapath design, control, memory. It also introduces students to several design entry methods including schematic capture and Hardware Description Languages using VHDL. The course also introduces Field Programmable Gate Arrays (FPGAs) as

a means to realize digital circuits using Xilinx CAD tools.

- **ENGG*3380, Computer Organization:** This course provides detailed examination of modern computer organization and techniques for microprocessor architecture design. Topics include - CPU design; instruction set design, addressing modes, operands; data flow design: internal bus structure, data flow signals, registers; control sequence design: hardwired control, decoding, micro-programming; architecture classes: CISC, RISC, and DSP; Memory organization; performance. Students must complete a term project that includes design, implementation, and demonstration of a CPU using a hardware descriptive language like VHDL.

Several other courses in the curriculum expand on ENG3050:

- **ENGG*4550, Advanced Computer Architecture:** This course covers topics such as: basics of pipeline structure, advanced pipelining and instruction level parallelism, multiprocessor and thread-level parallelism, memory-hierarchy design (main memory, virtual memory, caches), storage systems, interconnection networks, multiprocessor architectures (centralized and distributed). Advanced topics related to new emerging computer architectures will also be presented. The emphasis in each topic is on fundamental limitations and the trade-offs involved in designing computer systems, including memory and processing bandwidth, network bandwidth and latency, synchronization, and storage system bandwidth and latency.
- **ENGG*3190, Logic Synthesis:** This course presents automatic logic synthesis techniques for computer-aided design (CAD) of very large-scale integrated (VLSI) circuits and systems. Topics covered are: two-level Boolean network optimization, multi-level Boolean network optimization, technology mapping for library-based designs and field-programmable gate-array (FPGA) designs, and state-assignment and retiming for sequential circuits. The course will also cover various representations of Boolean functions such as binary decision diagrams (BDDs) and discuss their applications to logic synthesis.

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5 TEACHING AND LEARNING ACTIVITIES

5.1 Timetable

Lectures:				
Tuesday		16:00 - 17:20	MCKN 305	M. Abou El Nasr
Thursday		16:00 - 17:20	MCKN 305	M. Abou El Nasr
Laboratory:				
Friday	Sec 01	08:30 - 10:20	RICH 1532	M. Saunders

5.2 Lecture Schedule

Lectures	Lecture Topics	References	Learning Objectives
1-2	Introduction to Reconfigurable Computing	Chapter 1,2,3	1
3-4	Digital Design: Advanced Topics	Mano	1
5-6	Programmable Logic Devices (FPGAs, CPLDs)	Chapter 2,3	1,2,3
7-9	Hardware Descriptive Languages (VHDL)	Chapter 5,6	1,2,3,4
10-12	Hardware Descriptive Languages (VHDL)	Chapter 5,6	2,3,4,5
13-15	CAD for FPGAs (Placement, Routing, Synthesis)	Chapter 13,14	2,3,4,5
16-18	Hardware/Software Co-Design	Chapter 26	2,3,5
19-21	Electronic System Level (Vivadlo HLS)	Chapter 7	3,4,5
22-24	Dynamic Run-time Reconfiguration	Chapter 4	2,3,4,5
25-27	Application Specific Instruction Processors	Chapter 10	2,3,4,5
28-30	Operating Systems for RTR	Chapter 11	4,5
31-33	*Paper Review*	Papers	5
34-36	*RTR Applications & Course Review*	-	5

5.3 Lab Schedule

There will be 8 labs throughout the term. Below are the start and due dates:

Week	Topic	Weight	Report	Due
0	L0: Introduction to Lab Equipment and Safety	0%	None	-
1	L1: Design of a Complete Datapath	5%	Yes	Week 2
2	L2: Design of a Control Unit	10%	Yes	Week 3
3	L3: Design for Performance (Arithmetic Units)	15%	Yes	Week 4
4	L4: VHDL: Advanced Topics (Configurations)	10%	Yes	Week 5
5	L5: Xilinx System Generator (DSP)	10%	Yes	Week 6
6	L6: Design of Custom IP (H/S Co-design)	10%	Yes	Week 7
7	L7: Xilinx High Level Synthesis (HLS)	20%	Yes	Week 8
8	L8: Xilinx SDSoC (IP Integration)	20%	Yes	Week 10

5.4 Other Important Dates

1. Thursday, 6th September 2018: **First Class**.
2. Monday, 8th October 2018: **Thanks Giving Holiday**.
3. Tuesday, 9th October 2018: **No Classes Scheduled**.
4. Friday, 2rd November 2018: **Drop Date - 40th class day**.
5. Thursday, 29th November 2018: **Lecture** (Tuesday Schedule in Effect).
6. Friday, 30th November 2018: **Last Class** (Monday Schedule in Effect).

6 Lab Safety

Safety is critically important to the School and is the responsibility of all members of the School: faculty, staff and students. As a student in a lab course you are responsible for taking all reasonable safety precautions and following the lab safety rules specific to the lab you are working in. In addition, you are responsible for reporting all safety issues to the laboratory supervisor, GTA or faculty responsible.

7 Academic Misconduct

The University of Guelph is committed to upholding the highest standards of academic integrity and it is the responsibility of all members of the University community faculty, staff, and students to be aware of what constitutes academic misconduct and to do as much as possible to prevent academic offenses from occurring. University of Guelph students have the responsibility of abiding by the University's policy on academic misconduct regardless of their location of study; faculty, staff and students have the responsibility of supporting an environment that discourages misconduct. Students need to remain aware that instructors have access to and the right to use electronic and other means of detection.

Please note: Whether or not a student intended to commit academic misconduct is not relevant for a finding of guilt. Hurried or careless submission of assignments does not excuse students from responsibility for verifying the academic integrity of their work before submitting it. Students who are in any doubt as to whether an action on their part could be construed as an academic offense should consult with a faculty member.

7.1 Resources

The Academic Misconduct Policy is detailed in the Undergraduate Calendar:
http://www.uoguelph.ca/registrar/calendars/undergraduate/current/c08/c08-amisconduct.shtml

A tutorial on Academic Misconduct produced by the Learning Commons can be found at:
http://www.academicintegrity.uoguelph.ca/

Please also review the section on Academic Misconduct in your Engineering Program Guide.

The School of Engineering has adopted a Code of Ethics that can be found at:
http://www.uoguelph.ca/engineering/undergrad-counselling-ethics

8 Accessibility

The University of Guelph is committed to creating a barrier-free environment. Providing services for students is a shared responsibility among students, faculty and administrators. This relationship is based on respect of individual rights, the dignity of the individual and the University community's shared commitment to an open and supportive learning environment. Students requiring service or accommodation, whether due to an identified, ongoing disability for a short-term disability should contact the Centre for Students with Disabilities as soon as possible

9 Recording of Materials

Presentations which are made in relation to course work-including lectures-cannot be recorded or copied without the permission of the presenter, whether the instructor, classmate or guest lecturer. Material recorded with permission is restricted to use for that course unless further permission is granted.

10 Resources

The Academic Calendars are the source of information about the University of Guelph's procedures, policies and regulations which apply to undergraduate, graduate and diploma programs:
http://www.uoguelph.ca/registrar/calendars/index.cfm?index